CSE 240A Winter 2012 Assignment 5

Due Thursday 15/3 (In class at start of lecture) Homework should be typed. Do not forget to put your name and staple all sheets together. Please state your assumptions. Please state anyone you receive help from in doing this homework other than the Instructor or the TA.

1. Prefetching
   a. Is prefetching more effective for single-issue statically scheduled processors or multiple issue dynamically scheduled processors? Why?
   b. When can hardware prefetching hurt performance?
   c. When can software prefetching hurt performance?

2. Consider a processor implementing Tomasulo’s algorithm with reservation stations and the reorder buffer scheme as described class. Assume infinite processor resources unless stated otherwise; e.g., infinite execution units and infinite reservation stations. Assume a perfect branch predictor and assume there are no data dependences in the instruction stream we are considering. Assume the maximum instruction fetch rate is 12 instructions per cycle. (The other stages in the pipeline have no constraints; e.g., the processor can decode an unbounded number of instructions per cycle.)
   a. Suppose all instructions take one cycle to execute and the processor has an infinite reorder buffer. What is the average instructions-per-cycle rate or IPC for this processor?
   b. Consider the system in part (a) except that now every 24th instruction is a load that misses in the cache and the miss latency is 300 cycles. What is the average instructions-per-cycle or IPC for this processor?
   c. Consider the system in part (b) except that now the reorder buffer size is 24 entries. What is the average IPC for this processor?
   d. If the IPC for part (c) is less than 12, then what is the smallest reorder buffer size for which the IPC will be 12 again (assume the reorder buffer size can only be a multiple of 12).

3. Are the following statements true or false? Briefly explain your answer.
   a. Pipelining increases the amount of dynamic energy expended per instruction.
   b. Pipelining increases the energy-delay product of a computation.
   c. Relative to machines without reorder buffers, machines with reorder buffers can bottleneck on code that cache misses frequently to DRAM.
   d. Tomasulo machines without reorder buffers cannot precisely handle page faults.
   e. In-order machines with aggressive compilers can get close to the performance of out-of-order machines for code that has easily predictable behavior.
   f. Out-of-order is better at hiding misses to L2 than it is at hiding misses to DRAM.

4. Exceptions vs Interrupts (Be concise in your explanations).
   a. Explain the differences between exceptions and interrupts.
   b. Explain the similarities of exceptions and interrupts.