CSE 240A Winter 2012 Assignment 4

Assigned 29/2 Due Tuesday 6/3 (In class at start of lecture) Homework should be typed. Do not forget to put your name and staple all sheets together. Please state your assumptions. Please state anyone you receive help from in doing this homework other than the Instructor or the TA.

1. It is observed in the following code that each iteration requires two loads (A[j], then A[j+1024]) and a store (A[j]), and the cache hit rate on the store is 0% due to conflict misses. Tell me everything you can conclude about the cache. Assume that elements of A[] each require 4 bytes.

   for (j=0; j<N; j++)
   {
   }

2. A byte addressable 16-bit address system has a 2-way set associative LRU cache. The tag store requires a total of 4352 bits of storage. What is the block size of the cache? Please show all your work. (Hint: 4352 = 17x2^k, What all does bits the tag store have?)

3. There are various ways to index and tag your cache in relation to your virtual memory system. Consider that you have the following information about your system:
   • Accessing the TLB: 2ns
   • Indexing the cache to access its data portion: 3ns
   • Indexing the tag array of the data cache: 2.5ns
   • Tag comparisons: 1ns
   • Multiplexing the output data: 0.5ns

   Assume that all other parts are insignificant to the access time of the cache.

   For the following configurations, calculate the amount of time it takes to get data from the cache on a load hit. Be sure to explain your answers; just writing down numbers won't get you credit even if they end up being correct.
   a. A physically-indexed, virtually-tagged cache
   b. A virtually-indexed, virtually-tagged cache
   c. A virtually-indexed, physically-tagged cache
   d. A physically-indexed, physically-tagged cache

4. Find via an Internet search the size, associativity, and block size of all caches on the Intel Core i7 (Nehalem).