CSE 240A Winter 2012 Assignment 3

Assigned 3/2 Due Thursday 9/2 (In class at start of lecture)
Homework should be typed. Do not forget to put your name and staple all sheets together.
Please state your assumptions.

1. Consider 2 branch predictors, a 2-level local history predictor (local history table indexed by PC, branch history table of predictors indexed by local history table entry), and a correlating predictor (branch history table indexed by only the global history register). In each case the BHT is the same size (indexed by the same number of bits). We also discover that for the following code, the 2-level local predictor predicts the loop back branch B perfectly (after it gets warmed up), while the correlating predictor does not. What do we know about the size of the BHT? Assume the branches do not conflict with each other in the prediction tables.

```
for (j=0;j<10,000;j++)
{
    for (i=0;i<7;i++) // seven iterations
    {
        if (A[i] = = 0) // branch A
        {
            ...
        } // loop back branch B
    } // Loop back branch C
```

2. Increasing the size of a branch predictor typically reduces the chances of "aliasing" -- two branches sharing the same predictor. Usually, sharing results in negative interference (decreased prediction accuracy), but sometimes it can result in positive interference. Assuming a PC-indexed table of 2-bit predictors,
   a. Give an example of two branches (eg, show the T, N patterns for each, and how they are interleaved) that would result in positive interference (increased overall prediction accuracy).
   b. Give an example of two branches that would result in negative interference.
   c. Explain why most of the time you would expect to see negative interference with real code.

3. Suppose that a machine with a 5-stage pipeline uses branch prediction (i.e., no branch delay slots). 15% of the instructions for a given test program are branches, of which 80% are correctly predicted. The other 20% of the branches suffer a 4-cycle mis-prediction penalty. (In other words, when the branch predictor predicts incorrectly, there are four instructions in the pipeline that must be discarded.)
   a. Assuming there are no other stalls, develop a formula for the number of cycles it will take to complete n lines of this program.
   b. Now suppose you are given the option of replacing this processor’s branch prediction scheme with a 1-cycle branch delay system (i.e. one branch delay slot after every branch). What percentage of the branch delay slots must be filled in order for the CPU with the branch-delay system to have better performance than the CPU described in question 3.

4. A memory system consists of a single level cache with an access time of 1ns and a hit rate of 0.95, and a main memory with an access time of 60 ns.
   a. What is the effective memory access time of this system?
   b. If doubling the cache size reduces the miss rate by 30% but increases the cache access time by 10%, what is the expected percentage improvement in the effective access time if we double the cache size from part a?

5. Below, we have given you four different sequences of addresses generated by a program running on a processor with a data cache. Cache hit ratio for each sequence is also shown below. Assuming that the cache is initially empty at the beginning of each sequence, find out the following parameters of the processor's data cache (ensure that you sufficiently explain your answer):
   • Associativity (1, 2, or 4 ways)
   • Block size (1, 2, 4, 8, 16, or 32 bytes)
   • Total cache size (256B, or 512B)
   • Replacement policy (LRU or FIFO)

Address Sequence 1: [0, 2, 4, 8, 16, 32] Hit Ratio: 0.33
Address Sequence 2: [0, 512, 1024, 1536, 2048, 1536, 1024, 512, 0] Hit Ratio: 0.33
Address Sequence 3: [0, 64, 128, 256, 512, 256, 128, 64, 0] Hit Ratio: 0.33
Address Sequence 4: [0, 512, 1024, 0, 1536, 0, 2048, 512] Hit Ratio: 0.25

Assumptions: all memory accesses are one byte accesses. All addresses are byte addresses.