DRAM
Dynamic Random Access Memory (DRAM)

• Storage
  • Charge on a capacitor
  • Decays over time (us-scale)
  • This is the “dynamic” part.
  • About $6F^2$: 20x better than SRAM

• Reading
  • Precharge
  • Assert word line
  • Sense output
  • Refresh data

Only one bit line is read at a time. The other bit line serves as a reference. The bit cells attached to Wordline 1 are not shown.
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![Diagram of DRAM memory cells](image-url)

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DRAM: Write and Refresh

- **Writing**
  - Turn on the wordline
  - Override the sense amp.

- **Refresh**
  - Every few micro-seconds, read and re-write every bit.
  - Consumes power
  - Takes time

[Diagram of DRAM cell with wordlines and bitlines]
DRAM Lithography
Accessing DRAM

• Apply the row address
  • “opens a page”
  • Slow (~12ns read + 24 ns precharge)
• Contents in a “row buffer”
• Apply one or more column addr
  • fast (~3ns)
• Reads and/or writes
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```
One DD3 DRAM bank

<table>
<thead>
<tr>
<th>High order bits</th>
<th>Low order bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Row decoder</td>
<td>Column decoder</td>
</tr>
<tr>
<td>DRAM array</td>
<td></td>
</tr>
<tr>
<td>Sense Amps</td>
<td></td>
</tr>
<tr>
<td>Row Buffer</td>
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</table>

8K bits

Row Address
```

- 16k Rows
- One DD3 DRAM bank
- 8K bits
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DRAM Devices

- There are many banks per die (16 at left)
  - Multiple pages can be open at once.
  - Can keep pages open longer
  - Parallelism

- Example
  - open bank 1, row 4
  - open bank 2, row 7
  - open bank 3, row 10
  - read bank 1, column 8
  - read bank 2, column 32
  - ...

Micron 78nm 1Gb DDR3
DRAM: Micron MT47H512M4
DRAM: Micron
MT47H512M4
DRAM Variants

• The basic DRAM technology has been wrapped in several different interfaces.
  • SDRAM (synchronous)
  • DDR SDRAM (double data-rate)
    • Data clocked on rising and falling edge of the clock.
  • DDR2
  • DDR3
  • GDDR2-5 -- For graphics cards.
DDR3 SDRAM

- DIMM data path is 64bits (72 with ECC)
- Data rate: up to 1066Mhz DDR (2133Mhz effective)
- Bandwidth per DIMM GTNE: 16GB/s
  - guaranteed not to exceed
- Multiple DIMMs can attach to a bus
  - Reduces bandwidth/GB (a good idea?)

Each chip provides one 8-bit slice.
The chips are all synchronized and received the same commands.
Power

- DRAM is a major power sink.
-Idle power: 2-4W/DIMM
-Active power: 5-8W/DIMM

Economou, et. al 2006
DRAM Scaling

- Long term need for performance has driven DRAM hard
  - complex interface.
  - High performance
  - High power.
- DRAM used to be the main driver for process scaling, now it’s flash.
- Power is now a major concern.
- Scaling is expected to match CMOS tech scaling
- $F^2$ cell size will probably not decrease
- Historical foot note: Intel got its start as a DRAM company, but got out of it when it became a commodity.