Today

- IO
- TA Evaluations
Key Points

- CPU interface and interaction with IO devices
- The basic structure of the IO system (north bridge, south bridge, etc.)
- The key advantages of high speed serial lines.
- The benefits of scalability and flexibility in IO interfaces
- Disks
  - Rotational delay vs seek delay
  - Disks are slow.
  - Techniques for making disks faster.
- Flash and SSDs
  - How does flash memory store bits
  - How do you turn flash memory into a usable disk?
  - Why is that hard?
IO Devices

- Large Hadron Collider: 700MB/s
- Hard drive: 50-120MB/s
- Keyboard: 10Byte/s
- 30in display: 60Hz, 1GB/s
- 30in display: 60Hz, 1GB/s
Hooking Things to Your (Parents’) Computer

- What do we want in an IO system?
- Communicate with the computer
- Reliability
- latency
- bandwidth
- versatility
- cheap
- Compatibility
- Awesome
- Hook up lots of stuff
- User friendly

- Energy efficient
- Fun!
- Simple
- Ergonomic
- Small
- Wireless -- very wireless
- Convenient
- Secure
- Cross-platform
- Portable
- Fashionable
What IO Should be

- Lots of devices
  - Keyboards -- slowest
  - Printers
  - Display
  - Disks
  - Network connection
  - Digital cameras
  - Scanners
  - Scientific equipment
- Easy to hook up
  - “Plug and play”
  - The fewer wires the better.
- Easy to make sw work
  - No drivers!
  - “just works”
- Performance
  - Fast!!!!
  - Low latency
  - High bandwidth
  - Low power
- Cost
  - Cheap
  - Low hw and sw development costs
The CPUs World View

- The only IO that CPUs do is load, store, and receive interrupts
- “Programmed IO”
  - IO devices export “control registers” that drives map into the kernels address space
  - loads and stores to those addresses change the values in the control registers
  - Those address had better write through and/or uncached
  - Fine for small scale accesses, but PIO is usually slow.
- Direct memory access
  - The CPU is slow for moving bytes around, and it’s busy too!
  - DMA allows devices directly read and write memory
  - Fill a buffer with some data, start the DMA (via PIO), go do other things.
Interrupts

- IO devices need to get the CPUs attention
  - A DMA finishes
  - A packet arrives
  - A timer goes off

- (simplified) interrupt handling
  - CPU control transfers to the OS -- pipeline flush.
  - Like a context switch or a system call
  - Where control lands depends on the ‘interrupt vector’
  - The OS examines the system state to determine what the interrupt meant and processes it accordingly.
    - Copies data out of disk buffer or network buffer
    - Delivers signal to applications
    - etc.
Connecting Devices to Processors -- on chip

- Fastest possible connection.
- Wide -- you can have lots of wires between devices.
- Fast -- data moves at core clock speeds.
- Cheap -- fewer chips means cheaper systems.
- Restricts flexibility -- Design is set at fab time.
- Current uses -- L2 caches, on-chip memory controller, and (recently) GPUs.

Intel’s latest “Sandybridge” processor.
The “Chip set”

- Off-chip is much slower.
  - Fewer wires, slower clocks (less bandwidth), and longer latency.
- North Bridge - The fast part
  - “Front side bus” in Intel-speak
  - PCI-express
  - Key system differentiator until recently.
    - Server chip sets vs desktop chip sets
  - Memory-like interface
  - Typically 64bits of data
  - Routes PIO requests to other devices
  - Lots of DMA
    - It’s sort of a data movement co-processor
  - >64GB/s of peak aggregate bandwidth
The “Chip set”

- The South bridge -- the slow part
  - Everything else...
  - USB
  - Disk IO
  - Power management
  - Real time clock
  - System status monitoring -- i2c bus
  - 100s of MB/s of bandwidth
Core2 Duo Chipset

- Intel Core™2 Duo Processor
- PCI Express x16 Graphics
- 10 Hi-Speed USB 2.0 Ports; Dual EHCI: USB disable
- 6 PCI Express® x1
- Intel® Integrated 10/100/1000 MAC
- Intel® GbE LAN Connect
- Intel® High Definition Audio
- Intel® Quiet System Technology
- Intel® Matrix Storage Technology
- 6 Serial ATA Ports
- P965 MCH
- DDR2
- Intel® Fast Memory Access
- DMI
- LPC or SPI
- BIOS Support
- 8.5 GB/s
- 8 GB/s
- 12.8 GB/s
- 60 MB/s
- 500 MB/s each x1
- 3 Gb/s each
- Optional
Nehalem Chipset

X58 IOH
North bridge

South bridge
ICH10
ICH10R

Intel Core i7 Processor family
QPI 25.6 GB/s

DDR3 memory 8.5 Gb/s

PCI Express 2.0
Graphics Support for Multi-card configurations: 1x16, 2x16, 4x8 or other combination

12 Hi-Speed USB 2.0 Ports; Dual EHCI; USB

6 PCI Express x1

Intel Integrated 10/100/1000 MAC
GLCI LCI

Intel Gigabit LAN Connect

480 Mb/s each

500 MB/s each x1

2 GB/s DMI

up to 36 lanes

6 Serial ATA Ports; eSATA; Port Disable

Intel High Definition Audio

Intel Matrix Storage Technology

Intel Turbo Memory with User

Optional

LPC or SPI
BIOS Support

Intel Extreme Tuning Support
IO Interfaces

- **Protocol Layer**
  - What commands are legal and when?
  - What do they mean?

- **Transport Layer**
  - How do you send a chunk of data?
  - Negotiating access?

- **Physical Layer**
  - How do you send a bit?
  - What shape should connector be?
  - Voltage level?

- The protocol layer is largely independent of the lower layers
  - RS232 over USB
  - “IP over everything and everything over IP”
  - USB hard drives use the SCSI command set