NO EXPONENTIAL IS FOREVER . . .

Gordon E. Moore
Worldwide Semiconductor Revenues

Source: Intel/WSTS, 12/02
Average Transistor Price By Year

Source: Dataquest/Intel12/02
1" Wafer Of Planar Transistors, ~1959
The First Planar Integrated Circuit, 1961
1965 Transistor Projection
Integrated Circuit Complexity

Transistors Per Die

1965 Actual Data
MOS Arrays
MOS Logic 1975 Actual Data
1975 Projection

Source: Intel
Integrated Circuit Complexity

Transistors Per Die

- 1965 Actual Data
- MOS Arrays
- MOS Logic 1975 Actual Data
- 1975 Projection
- Memory
- Microprocessor

Source: Intel
Projected 2000 Wafer, circa 1975

Moore was not always accurate
Combination of copper + low-k dielectric now meeting performance and manufacturing goals
Minimum Feature Size

** Examples

- Human hair, 100 µm
- Amoeba, 15 µm
- Red blood cell, 7 µm
- AIDS virus, 0.1 µm
- Buckyball, 0.001 µm

Feature Size (microns)

Intel [update 5/20/02]

ITRS [2001 edition]

** Planar Transistor; remaining data points are ICs.

Source: Intel, post '96 trend data provided by SIA

International Technology Roadmap for Semiconductors (ITRS)

^ [ITRS DRAM Half-Pitch vs. Intel "Lithography"]
$1 \, \mu m^2$ SRAM Cell

P501 Contact 1978

P1262 SRAM Cell 2002

$1 \, \mu m$
50nm Resist Lines With 193nm Light

-0.2um focus

-0.3um focus

"best focus"

+0.2um focus

+0.3um focus
193nm Step and Scan Production Tool
Minimum Insulator Thickness vs Time

Oxide Thickness (Nanometers)

100
10
1

Source: Intel
High K for Gate Dielectrics

- 90nm process
  - Capacitance: 1X
  - Leakage: 1X

- Experimental high-k
  - Capacitance: 1.6X
  - Leakage: < 0.01X

Source: Intel
Processor Power (Watts) - Active & Leakage
New Materials and Device Structures
Extending Transistor Scaling

**Changes Made**
- Gate Silicide Added
- Channel Strained Silicon

**Future Options**
- High-k Gate Dielectric
- New Transistor Structure
Technology Generations to Come

Double the Density
Reduce Line Width by 0.7x

130nm ➔ 90nm ➔ 60nm ➔ 45nm ➔ 30nm ➔ ?

2 or 3 years between generations

~10 ± 2 Years
EUV Printed and Etched Lines

100 nm, $k_1 = 0.75$

80 nm, $k_1 = 0.60$

50 nm dense, $k_1 = 0.37$
Extreme Ultraviolet (EUV) Lithography
NO EXPONENTIAL IS FOREVER . . .

BUT

WE CAN DELAY “FOREVER”