

ISSCC2009 Keynote

**Adaptive Circuits
for
the 0.5-V Nanoscale CMOS Era**

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OUTLINE

1. Introduction

The 1-V wall

2. Adaptive Circuits for Memory-Rich LSIs

Trends in V_{min}

Breakthrough technologies

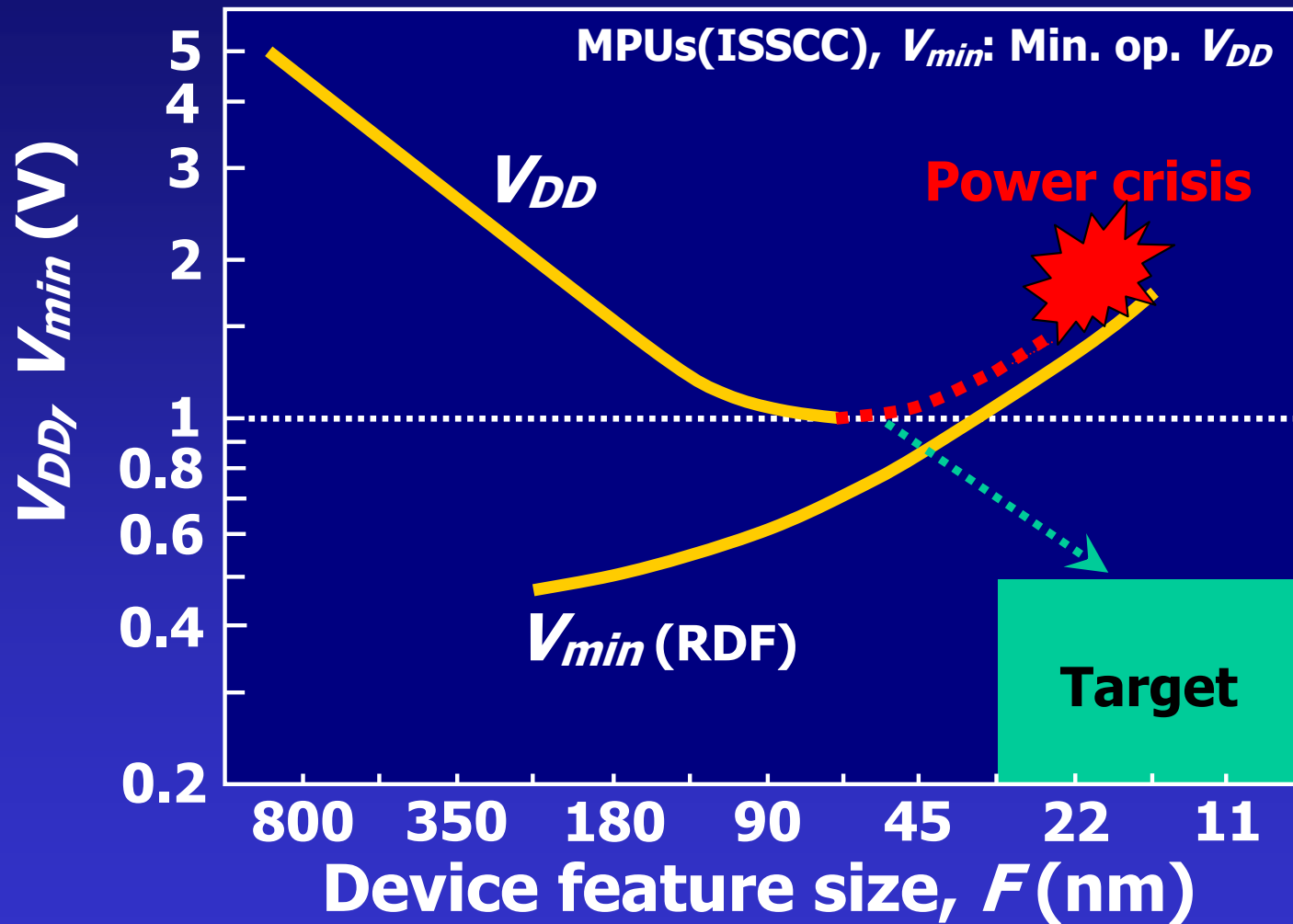
Scenario to the 0.5-V nanoscale era

3. Adaptive Circuits for Mixed Signal LSIs

Digital assisted analog design

4. Conclusion

The 1-V Wall



RDF: Random Dopant Fluctuation

What should we do to lower V_{DD} ?

1. Reduce min. operating V_{DD} (V_{min}) by reducing

- Lowest necessary V_t (V_{t0}),

- Intrinsic V_t -variation (ΔV_t).

→ New devices, circuits, repair etc.

2. Reduce power-supply noise (V_{ps})

→ Compact subsystems (small core/chip, 3-D chip stack) etc.

Reducing V_{min} is the key. ($V_{min} \gg V_{ps}$)

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3. Adaptive Circuits for Mixed Signal LSIs

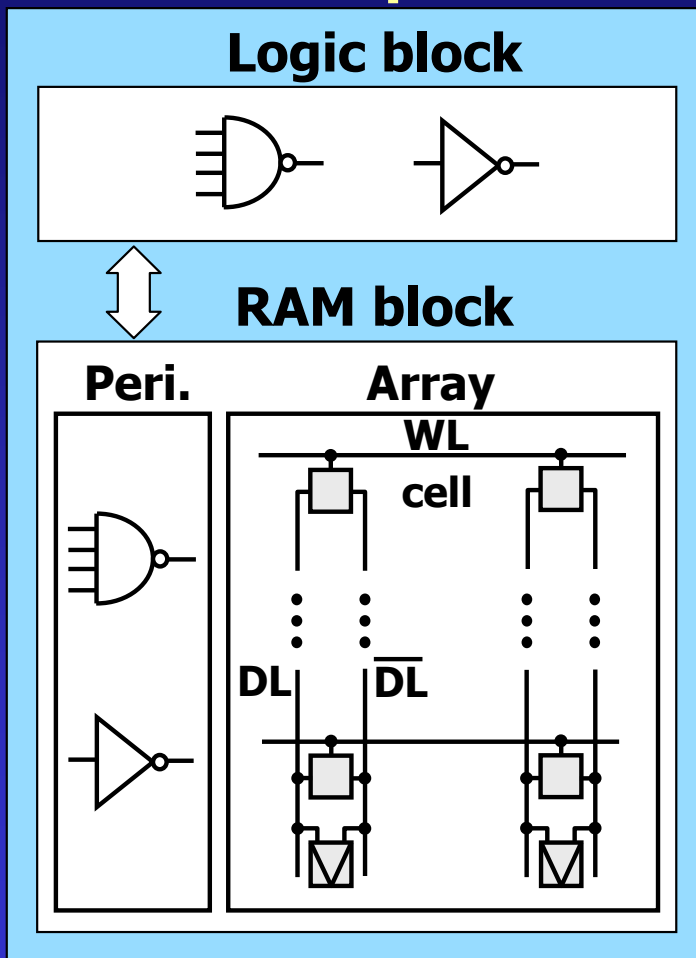
Digital assisted analog design

4. Conclusion

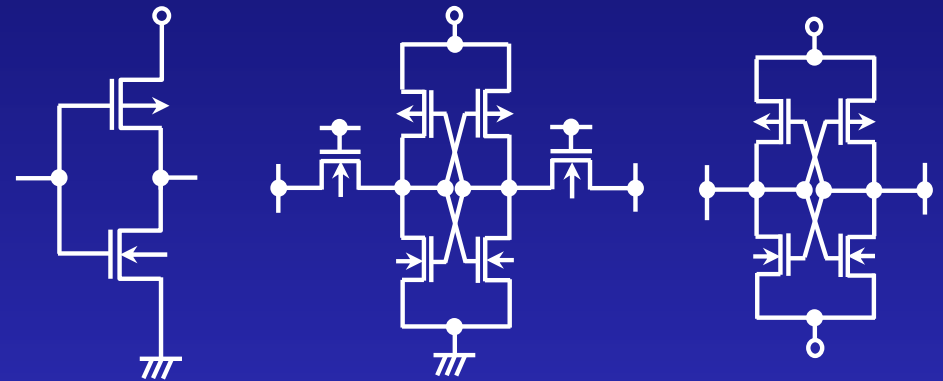
Circuits Giving Low- V_{DD} Limitations

* Most sensitive to ΔV_t

Chip



Inverter SRAM Cell* DRAM SA*

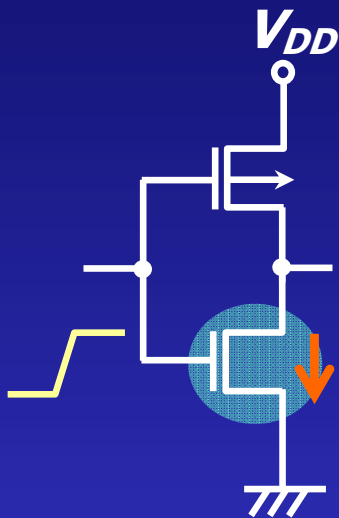


ΔV_t	large	largest	small
LW	$8F^2(\text{av.})$	$1.5-3F^2$	$15F^2$
Count	large	largest	medium

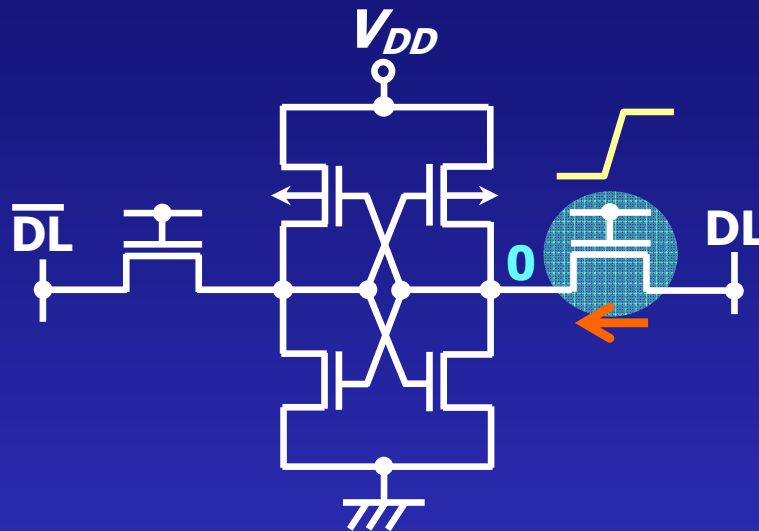
$$\Delta V_t \propto 1/\sqrt{LW}, \quad F: \text{device feature size}$$

Definition of V_{min}

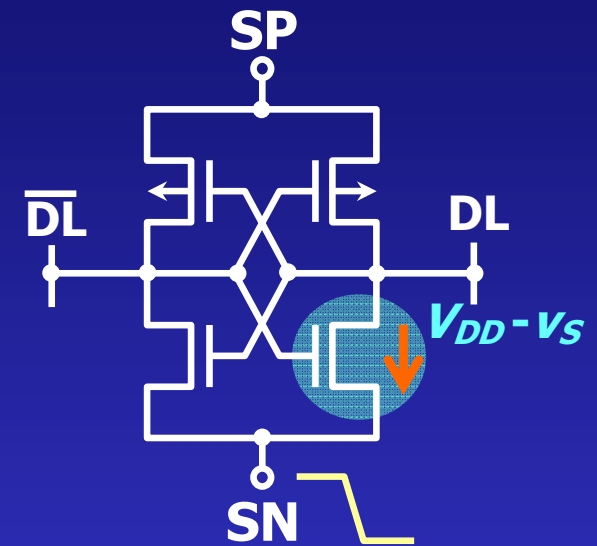
Inverter



SRAM Cell



DRAM SA



$$\tau(V_t) \propto V_{DD} / (V_{DD} - V_t)^{1.2}$$

$$\begin{aligned} \Delta\tau &= \tau(V_{t0} + \Delta V_{tmax}) / \tau(V_{t0}) \\ &= \left\{ (V_{DD} - V_{t0}) / (V_{DD} - V_{t0} - \Delta V_{tmax}) \right\}^{1.2} \end{aligned}$$

V_{t0} : Lowest necessary av. V_t

ΔV_{Tmax} : Max. variation in V_t

$$V_{min} = V_{DD} \text{ for a fixed } \Delta\tau$$

$$= V_{t0} + (1 + \gamma) \Delta V_{tmax}$$

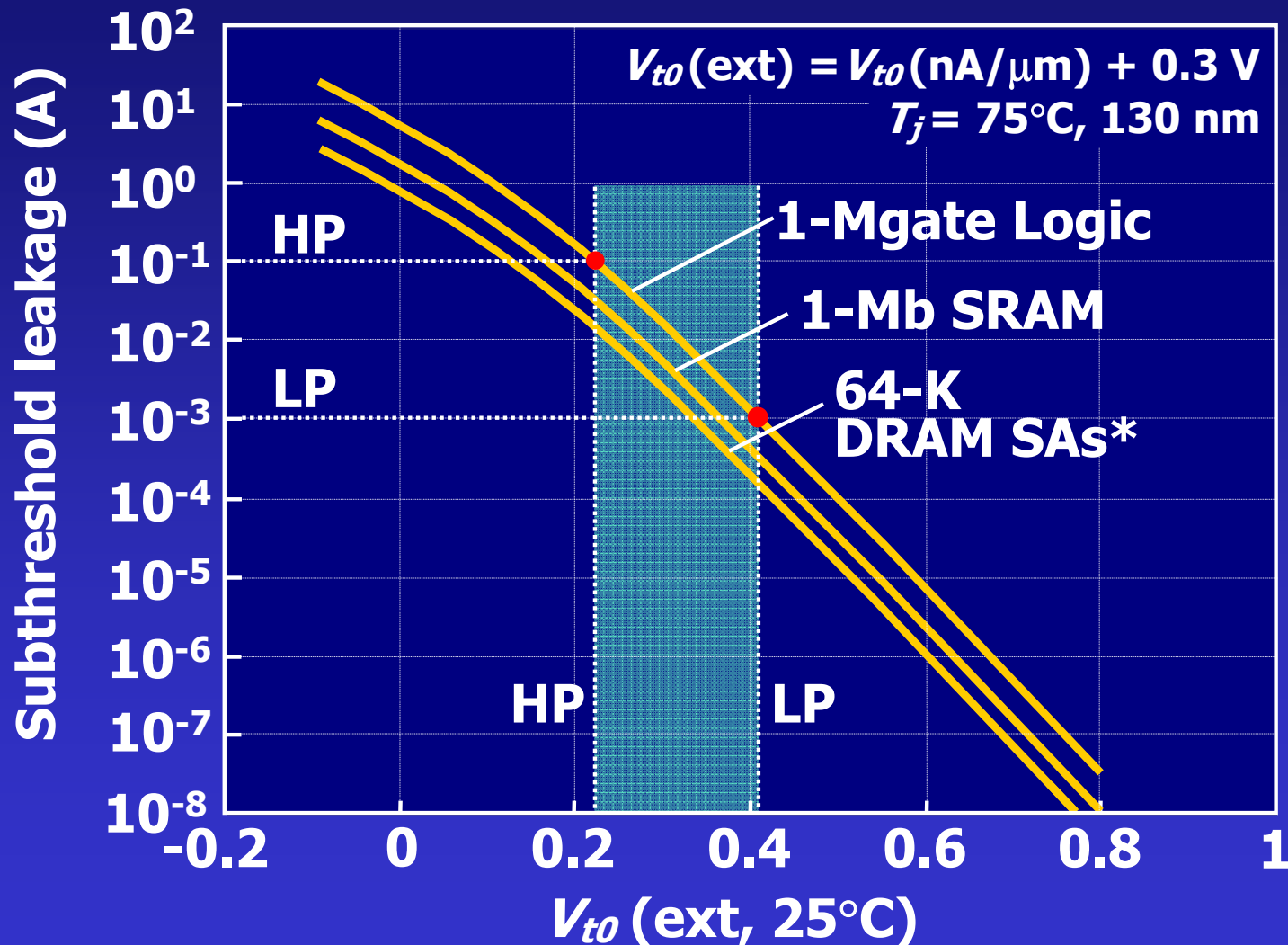
$$\gamma = 1 / (\Delta\tau^{1/1.2} - 1)$$

$\Delta\tau$: Tolerable speed variation

$$\gamma \cong 2-3 \text{ for } \Delta\tau = 1.4 - 1.6$$

High and Unscalable V_{t0}

HP: high performance, LP: low power



* contributing to leakage in active standby mode

ΔV_{tmax}

$$\Delta V_{tmax} = m\sigma$$

- $m \rightarrow$ circuit count

- $\sigma = A_{vt} / \sqrt{LW}$

$$\propto \{t_{ox}(V_{t0} + 0.1 \text{ V})\}^{0.5}$$

$$\propto N_{sub}^{0.25}$$

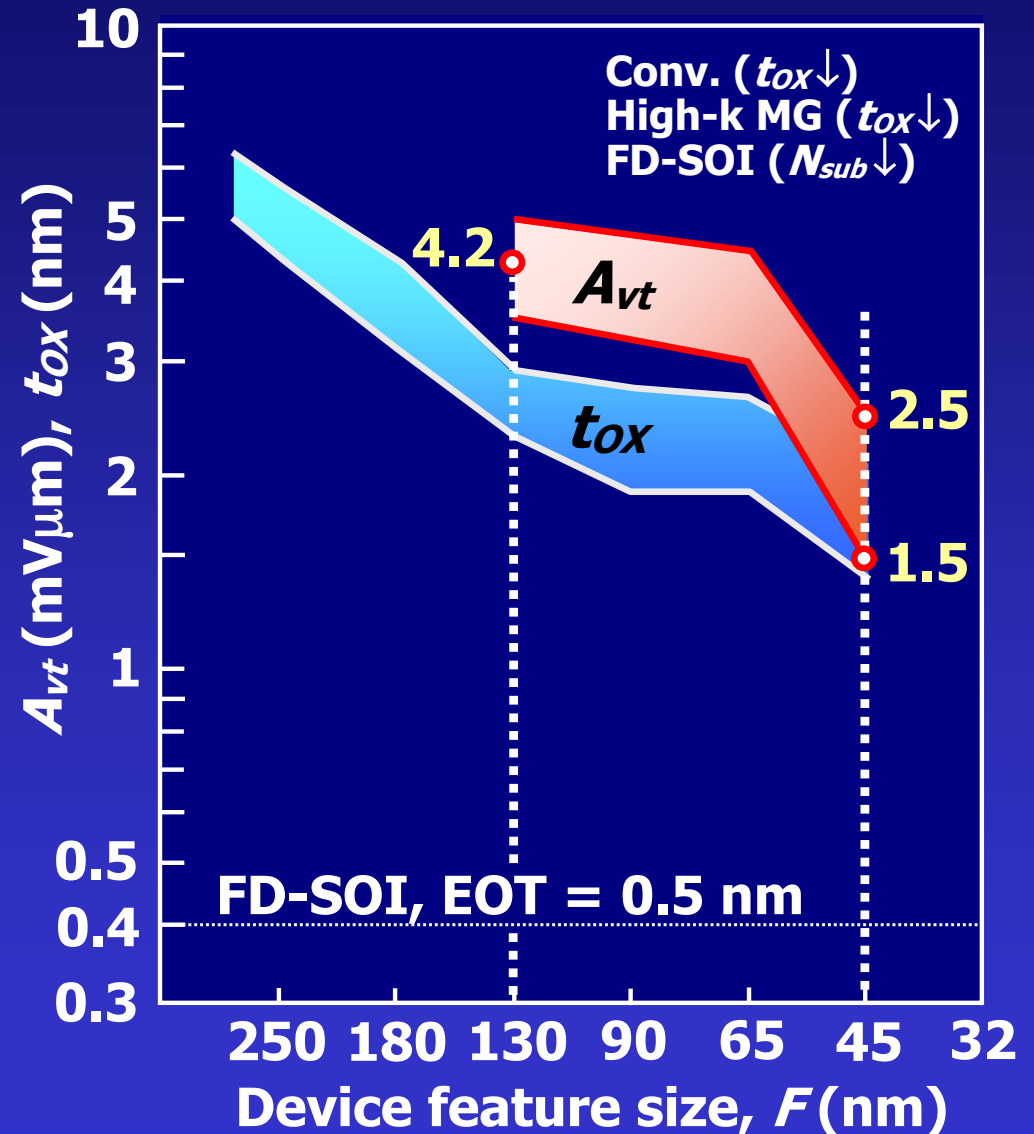
For lower ΔV_{tmax} , use

1. Repair

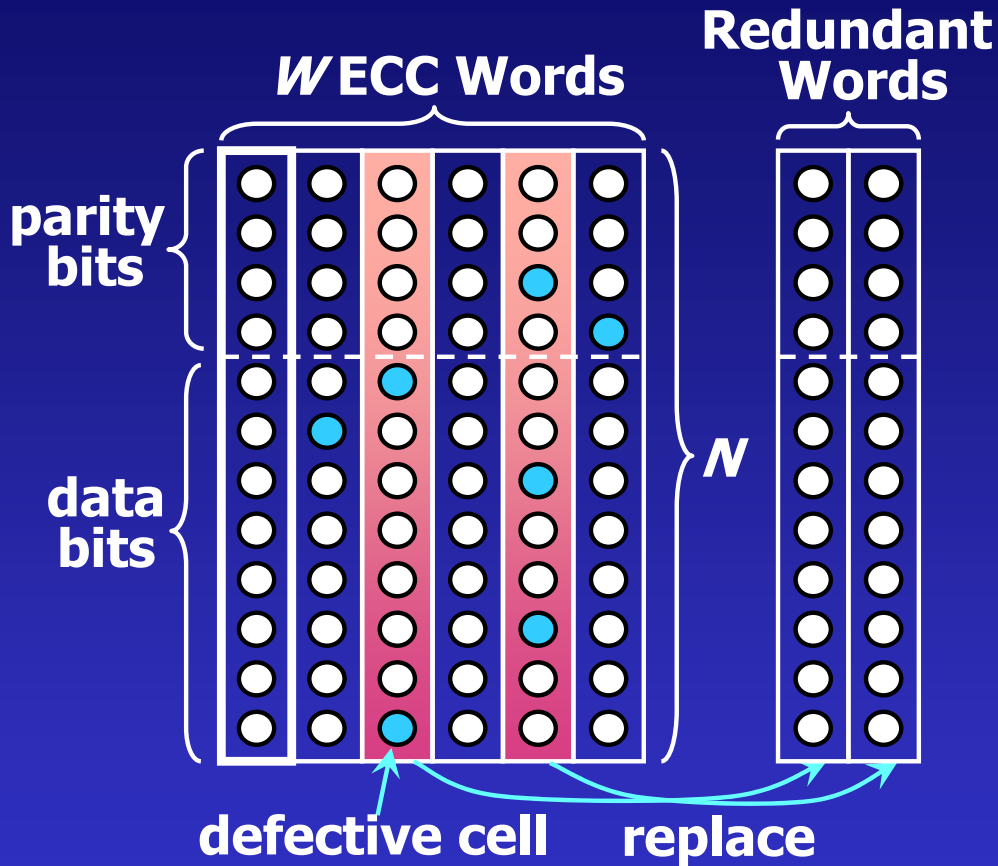
ECC + Redundancy ($m \rightarrow 1/2$)

2. Small σ technologies

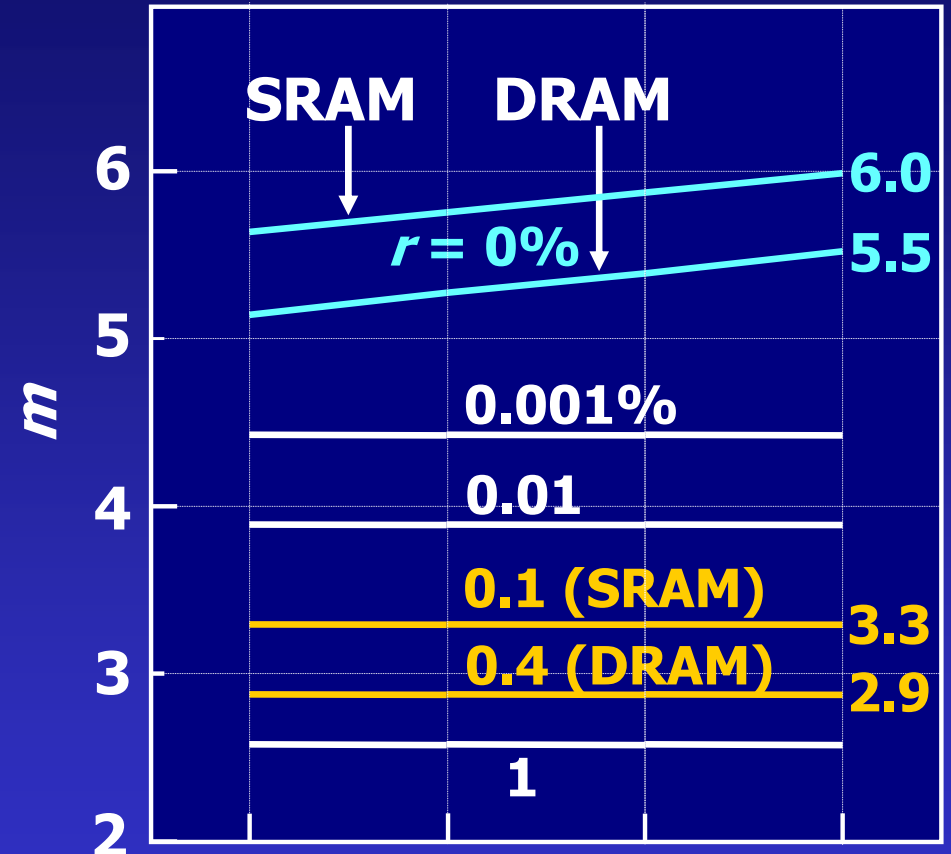
- Circuits tolerating
The largest MOSFET possible
The lowest V_{t0} possible
- Small- A_{vt} MOSFETs



ECC + Redundancy



- ECC word with one defect cell corrected by ECC.
- ECC word with two or more defect replaced by a redundant word.



SRAM(b) 32M 64M 128M 256M
 DRAM(b) 128M 256M 512M 1G

r: repairable %

Max *r* = 0.1%(SRAMs), 0.4%(DRAMs).

K. Itoh, ESSCIRC2007 Dig., pp. 68-75

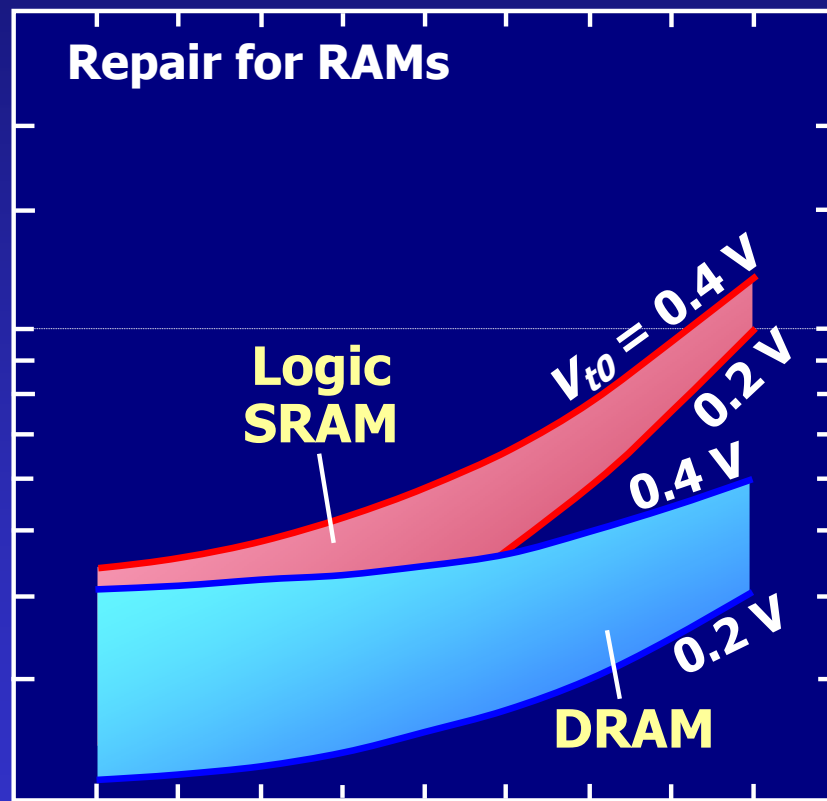
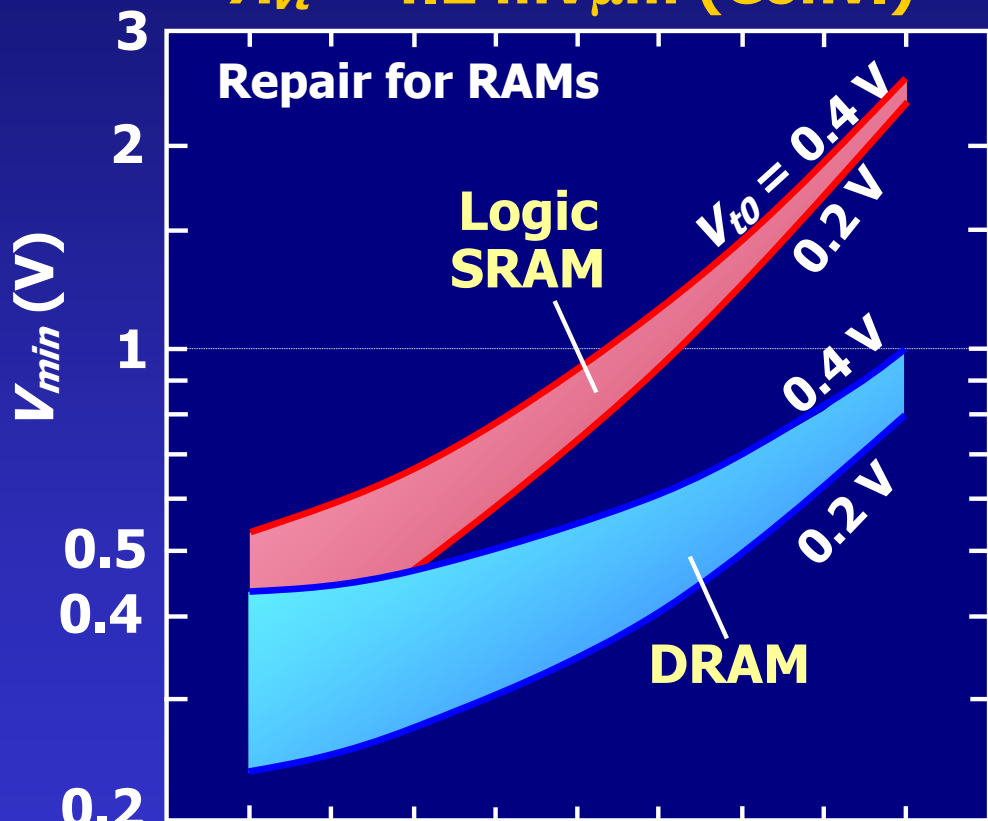
Trends in V_{min}

$$\sigma = A_{vt} / \sqrt{LW}$$

$$LW = 8F^2(L), 1.5F^2(\text{SRAM}), 15F^2(\text{DRAM})$$

$A_{vt} = 4.2 \text{ mV}\mu\text{m}$ (Conv.)

$A_{vt} = 1.5 \text{ mV}\mu\text{m}$ (Hi-k MG, SOI)

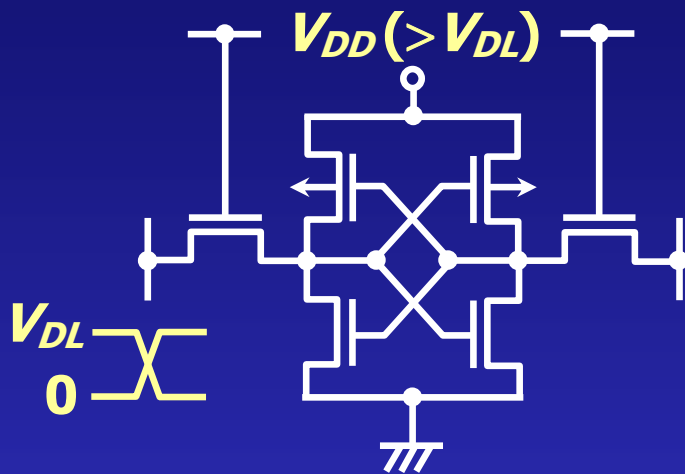


$F(\text{nm})$	250	180	130	90	65	45	32	22	15	11
Logic (g)	1.3M	5M	20M	80M	320M					
SRAM (b)	8M	32M	128M	512M	2G					
DRAM (b)	32M	128M	512M	2G	8G					

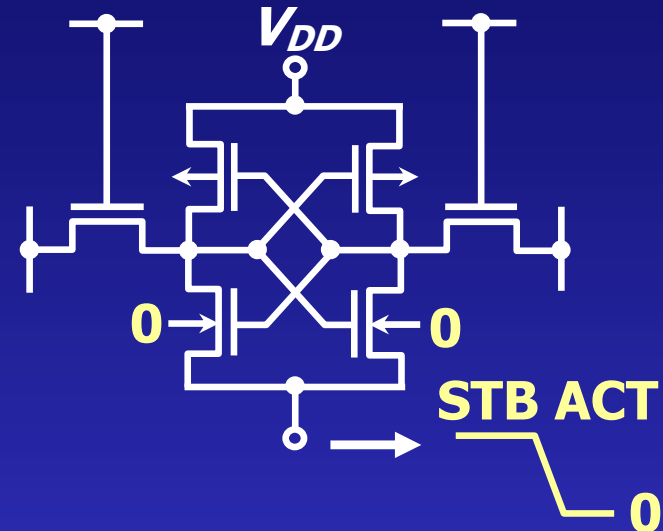
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State-of-the-Art SRAM Cells

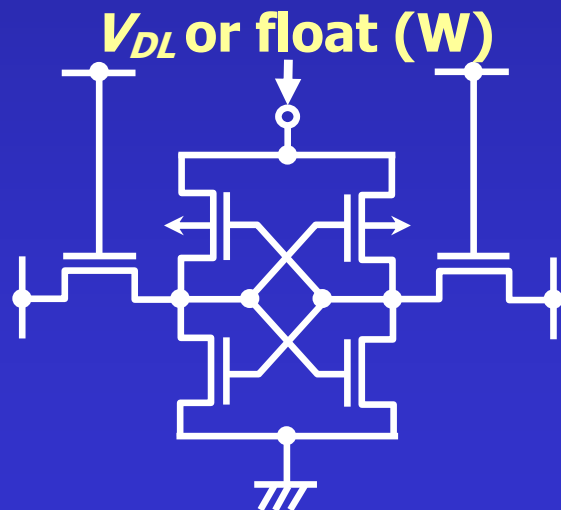
Increased cell-power supply



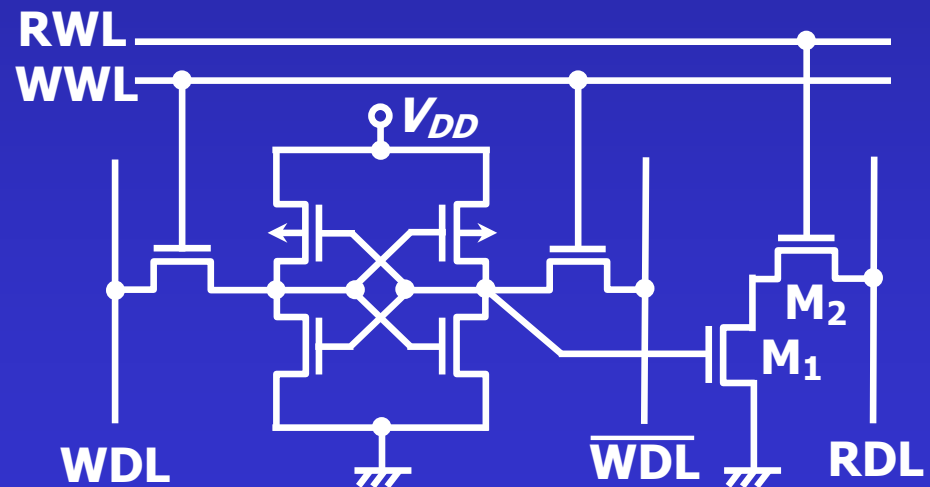
Dynamic S-control



Dynamic S-control



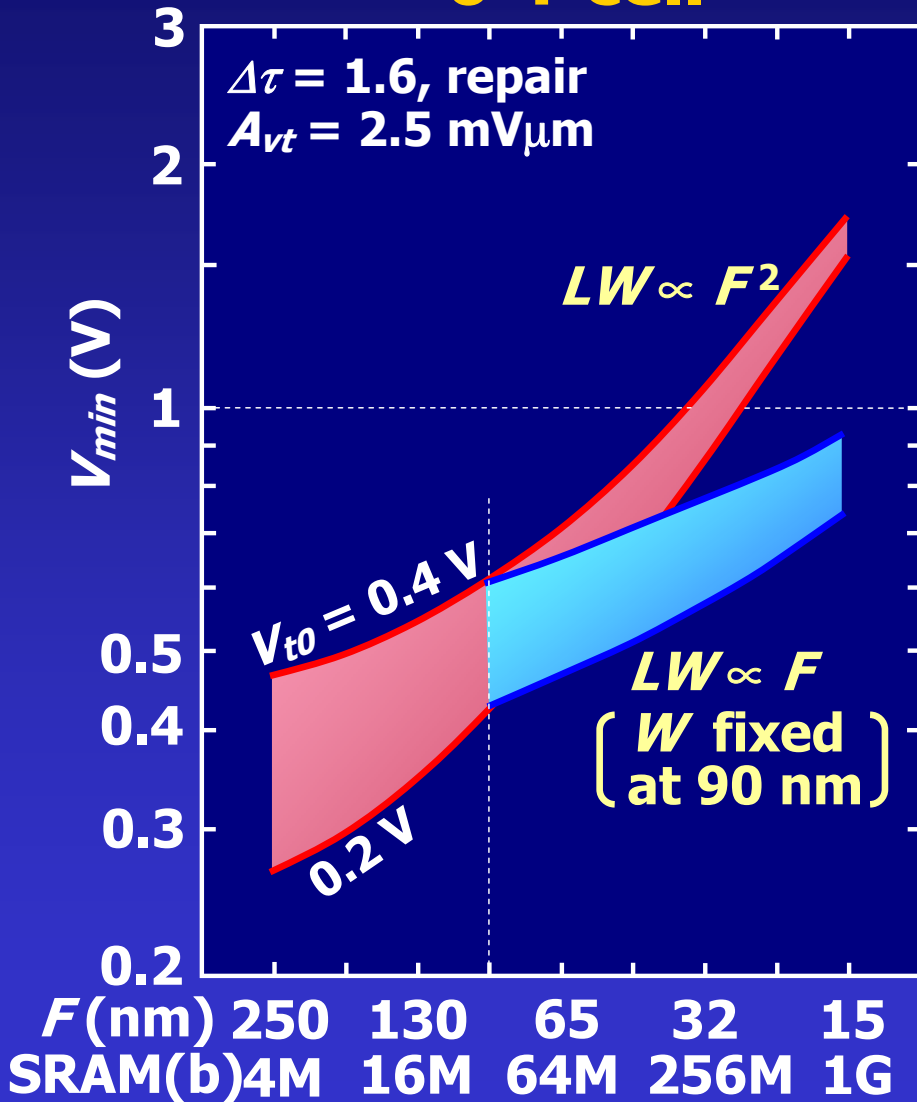
8-T cell



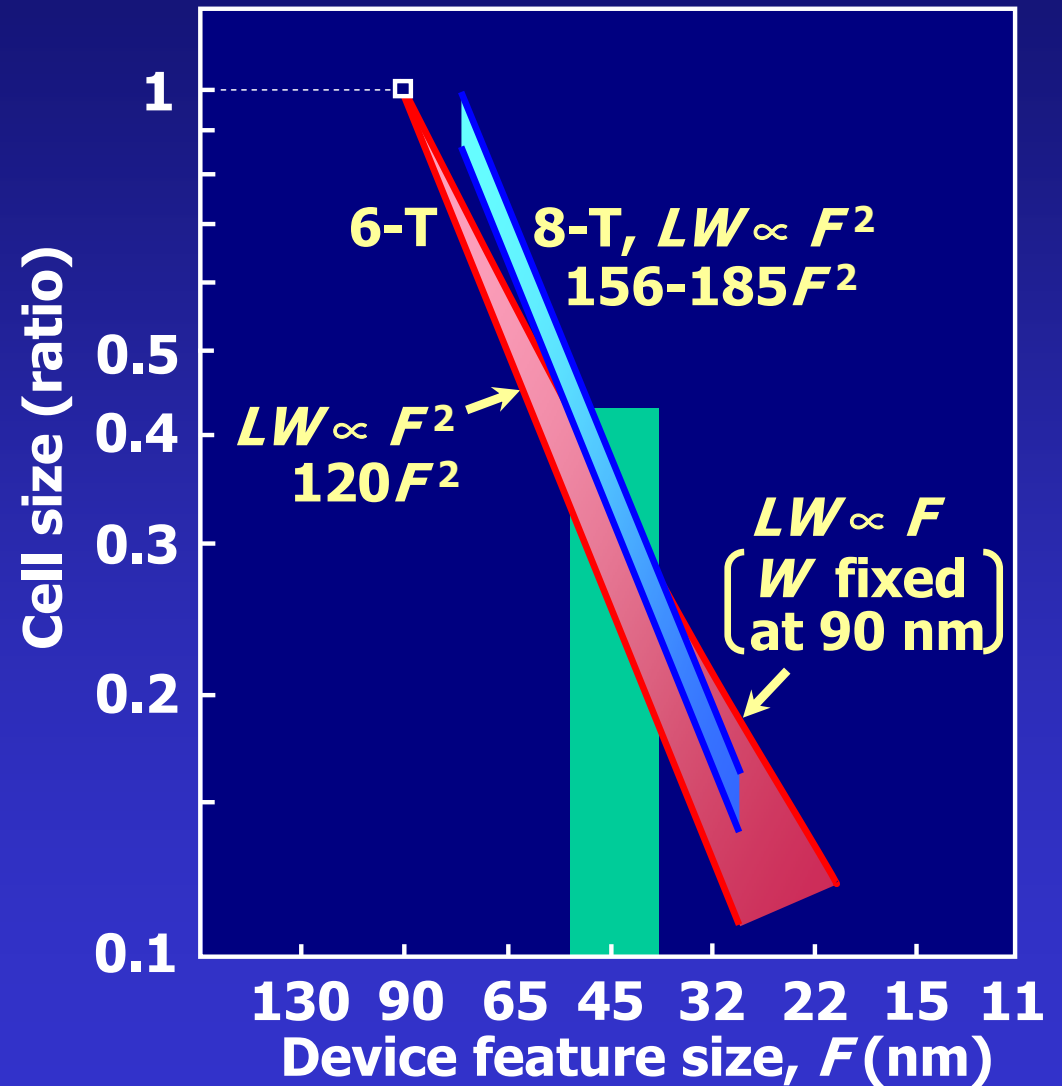
K. Itoh, p. 132, VLSI Circuits'96; H. Akamatsu, p. 14, VLSI Circuits'96; F. Hamzaoglu, ISSCC'08, p. 376; L. Chang, p. 252, VLSI Circuits'96

Reduction in V_{min} of SRAMs

6-T cell



6-T cell vs 8-T cell



Breakthrough Technologies

for reducing V_{min} and V_{ps}

The best way to predict the future is to invent it.

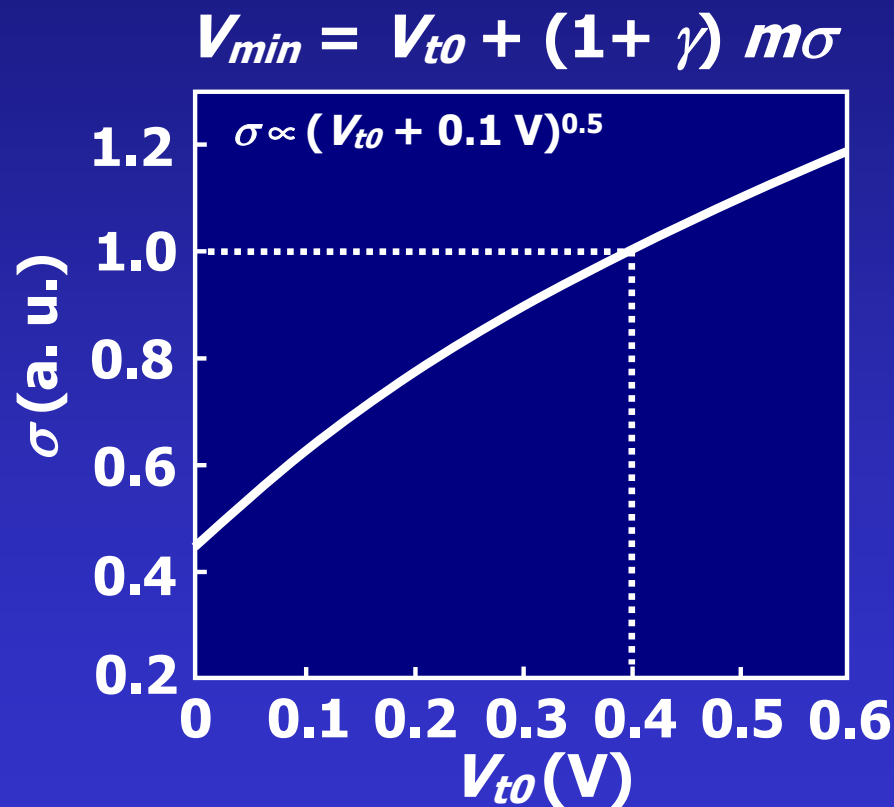
1. Adaptive devices/circuits

($V_{min} \downarrow$)

- σ -scalable FinFET
- Dual- V_{DD} dual- V_{t0} circuit

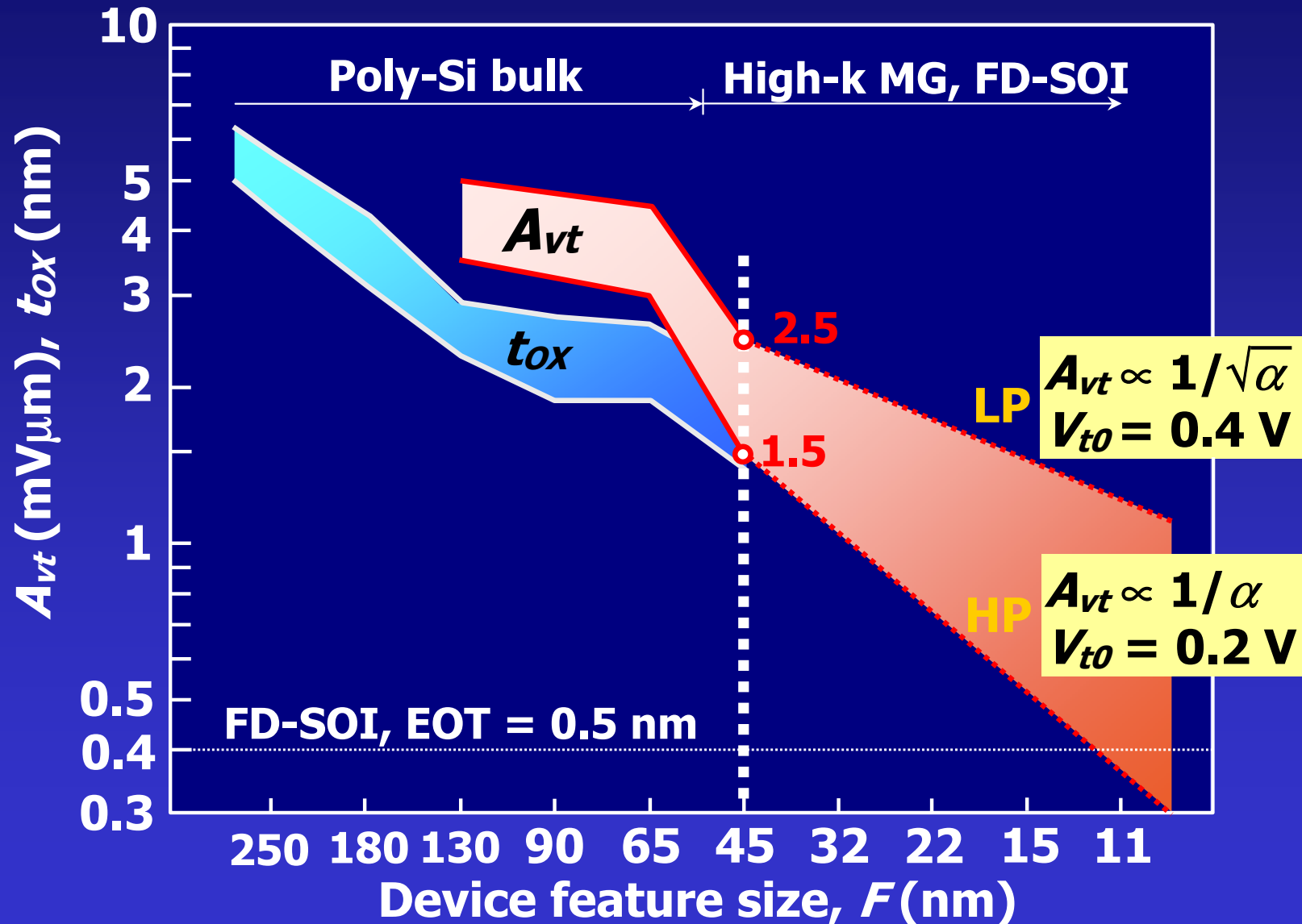
2. Adaptive tech. ($V_{ps} \downarrow$) with small chip/compact subsystem

- 2-D selection FinFET cell
- Many-core and chip stack



Assumptions for A_{vt} and V_{t0}

$$\sigma = A_{vt}/\sqrt{LW}, \alpha > 1 \quad (\alpha: \text{device scaling factor})$$



σ -Scalable FinFET

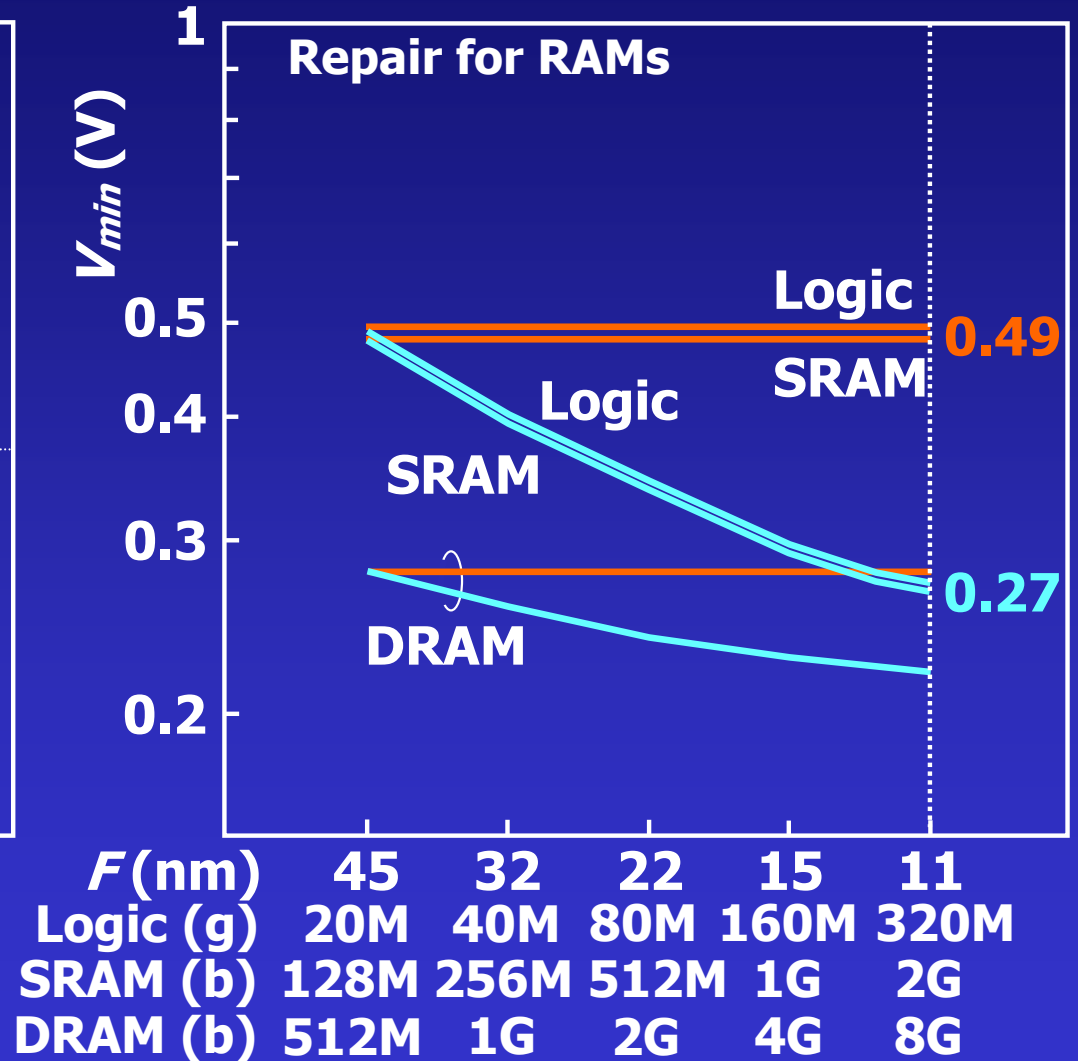
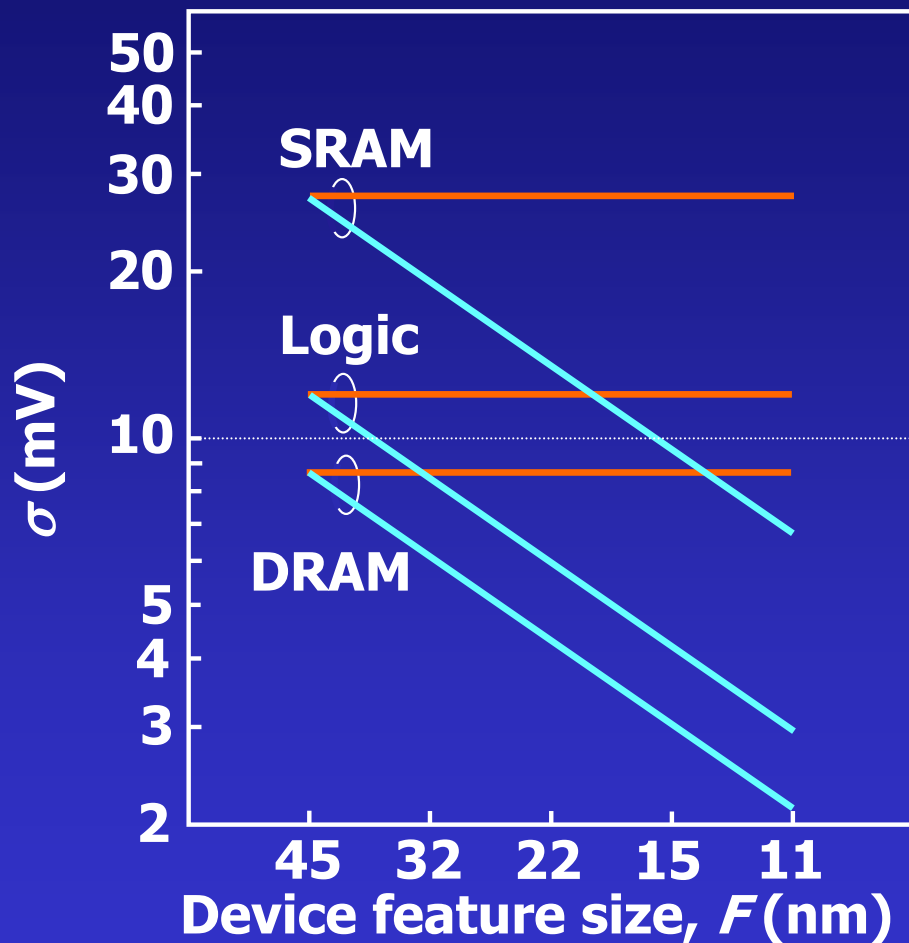
by scaling up the height of fin

	Planar		FinFET	
	HP	LP	HP	LP
σ	1	$\sqrt{\alpha}$	$1/\alpha$	$1/\sqrt{\alpha}$
A_{vt}	$1/\alpha$	$1/\sqrt{\alpha}$	$1/\alpha$	$1/\sqrt{\alpha}$
L	$1/\alpha$	$1/\alpha$	$1/\alpha$	$1/\alpha$
W	$1/\alpha$	$1/\alpha$	α	α
LW	$1/\alpha^2$	$1/\alpha^2$	1	1

$$\alpha > 1, \sigma = A_{vt} / \sqrt{LW}$$

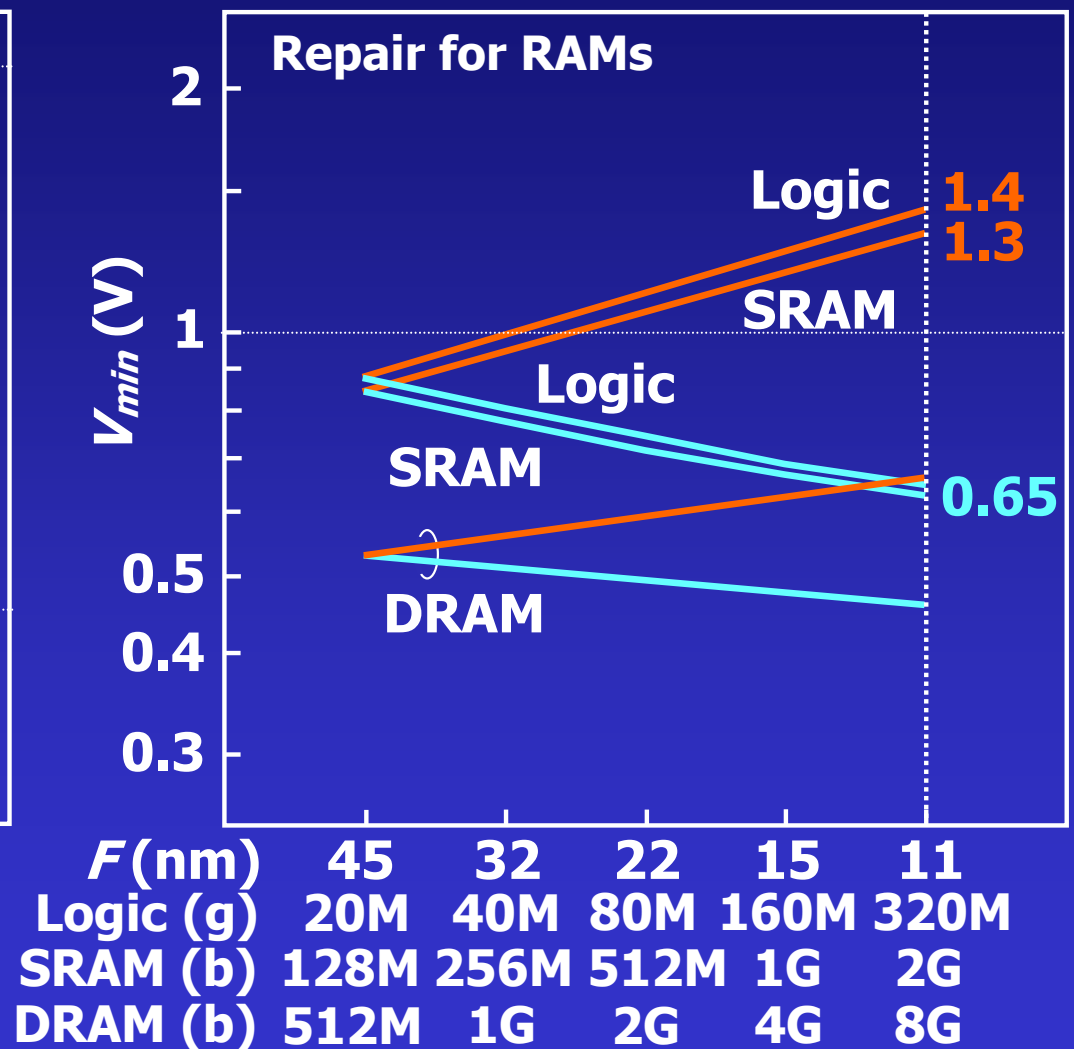
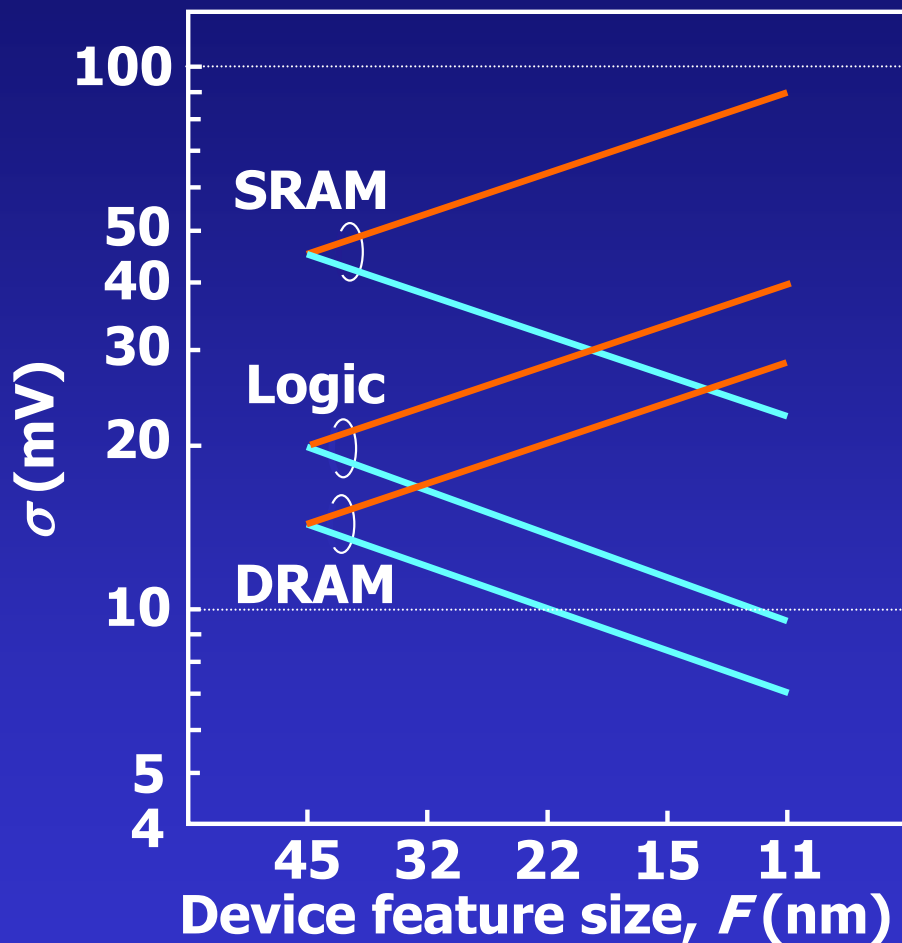
σ and V_{min} for HP Designs

— Planar — Fin

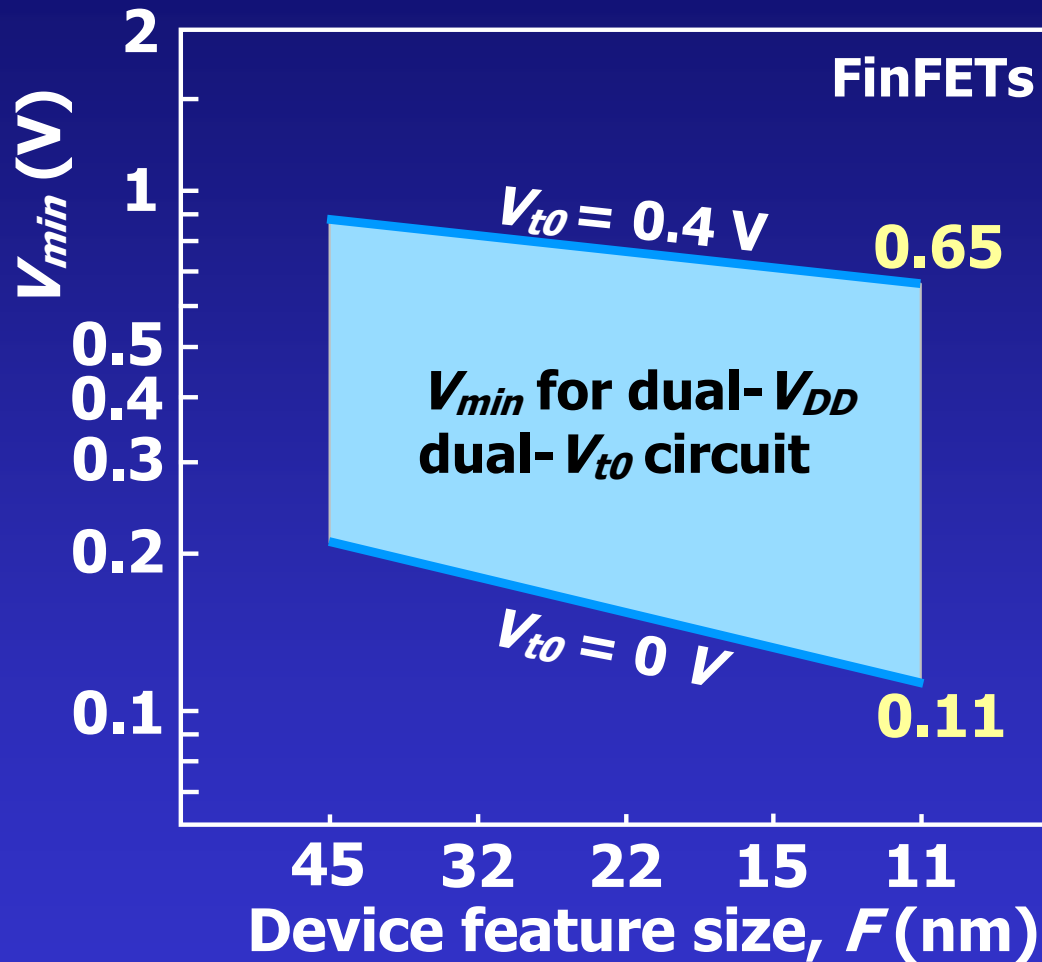


σ and V_{min} for LP Designs

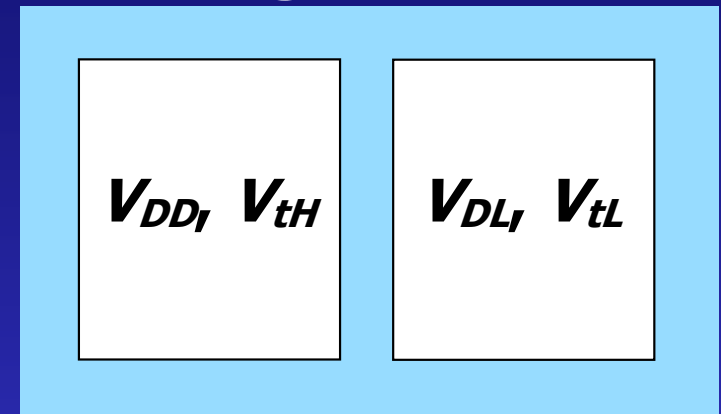
— Planar — Fin



Dual- V_{DD} Dual- V_{t0} Dynamic Circuit

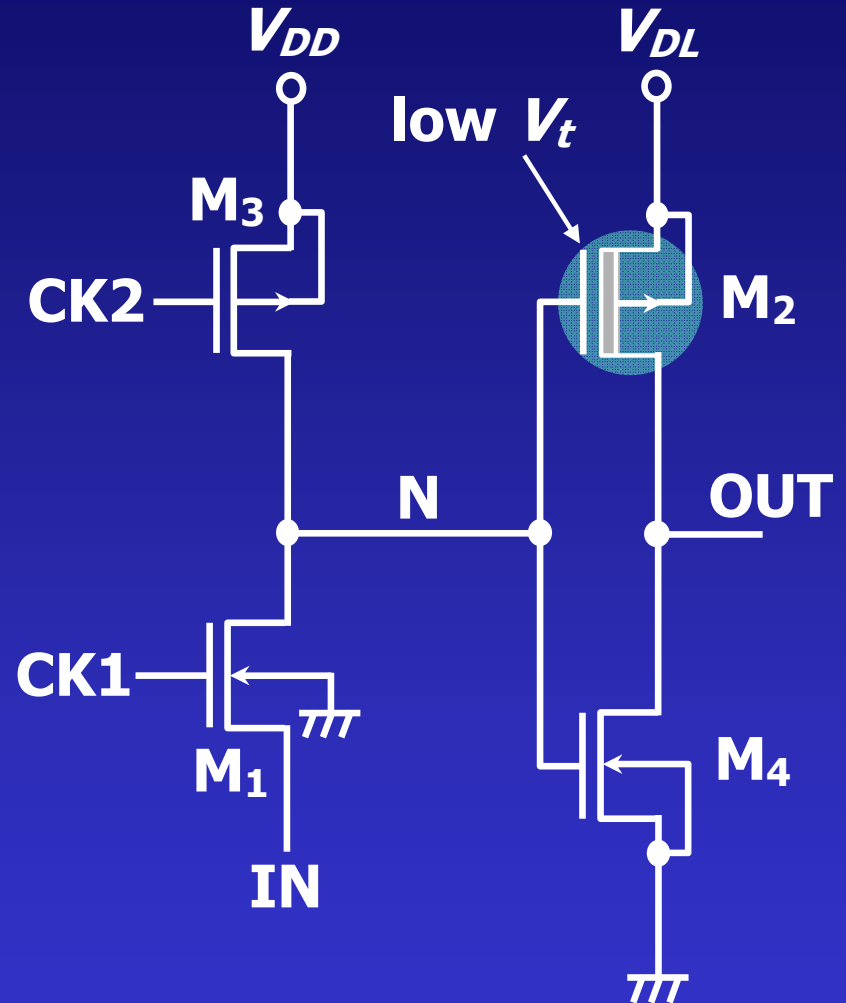
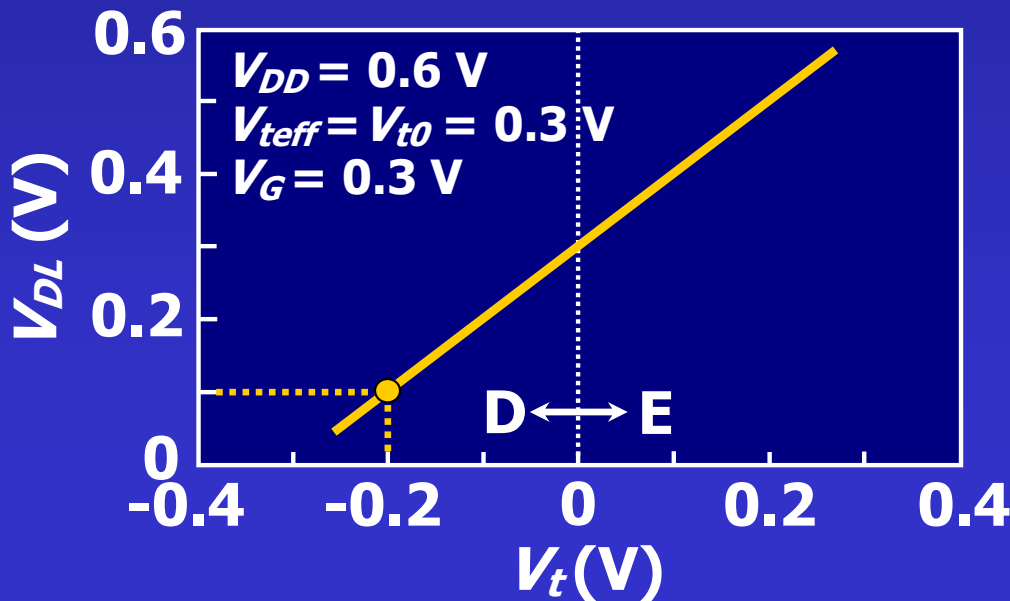
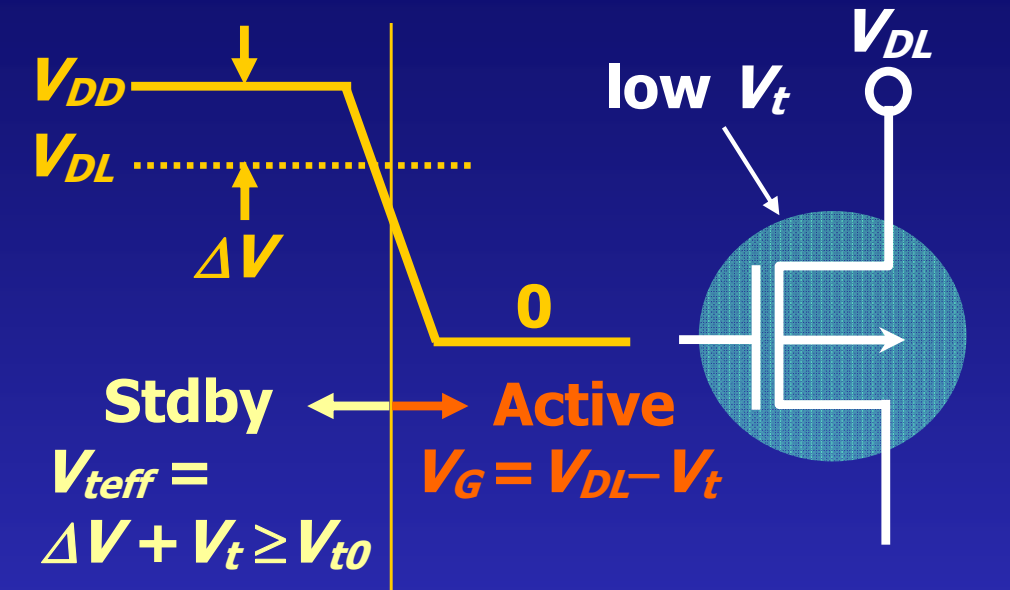


Logic block



Bigger area of V_{DL} sub-block
 \rightarrow Lower V_{min}

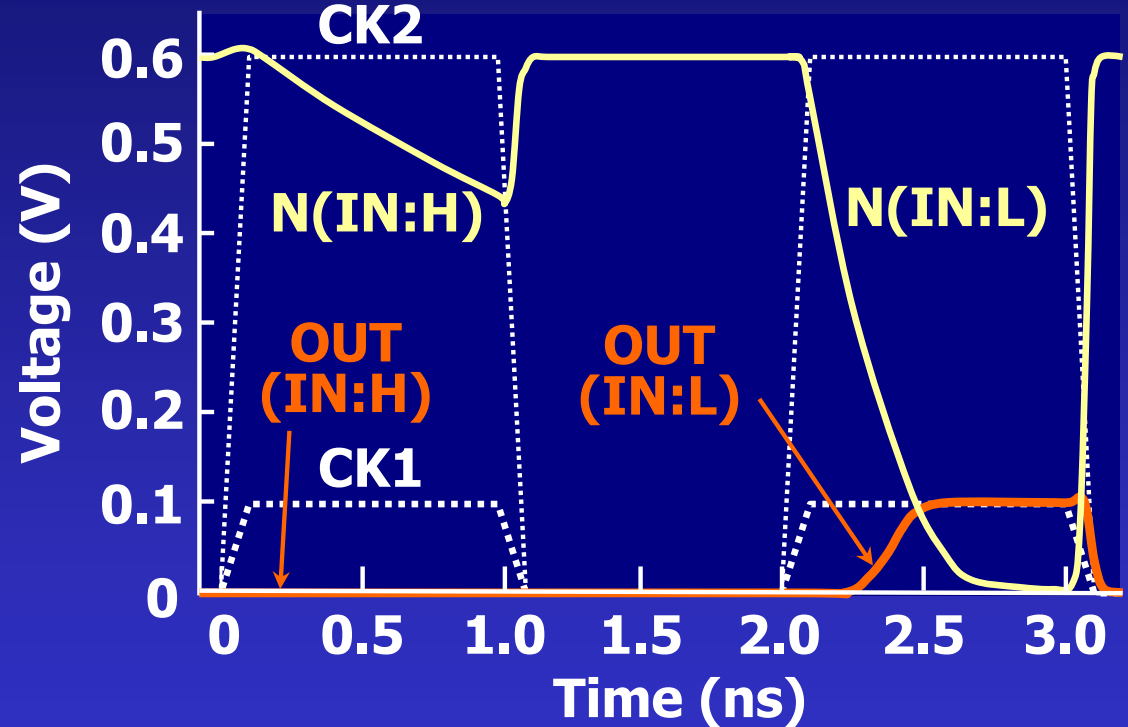
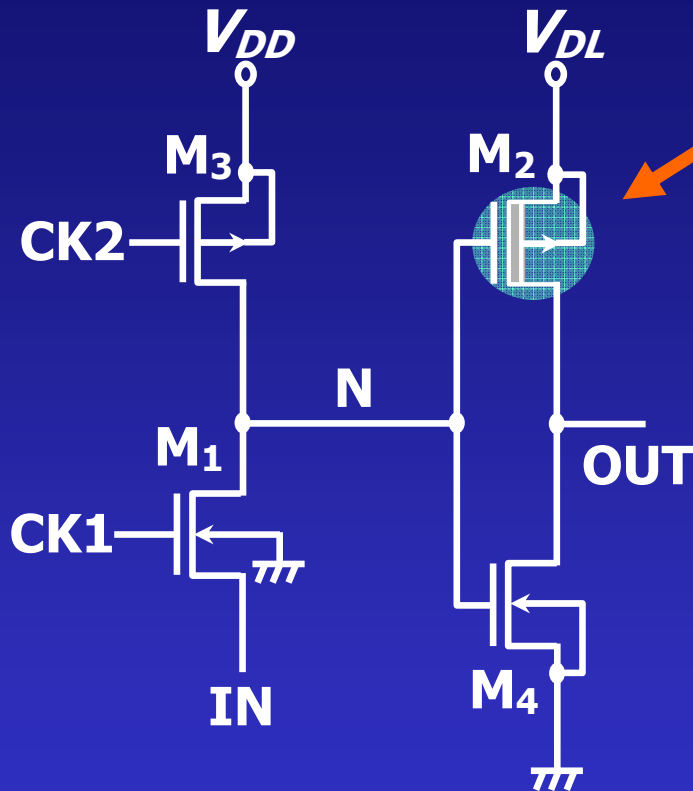
Gate-Source Offset Driving



K. Itoh et al., p. 68, ESSCIRC2007

0.1-V Swing E/D Dynamic Inverter

$V_{DL} = 0.1 \text{ V}$, $V_{DD} = 0.6 \text{ V}$
D-MOS ($V_t = 0.2 \text{ V}$)



Others: E-MOS ($V_t = 0.3 \text{ V}$).
 $W \text{ (nm)} = 140 \text{ (M}_1, \text{M}_3)$,
 $420 \text{ (M}_2)$, $280 \text{ (M}_4)$, $L = 50 \text{ nm}$
 $C_L = 4\text{fF} + 4\text{MOSs}$.

- **Widely applicable to low-power buffers and others.**

K. Itoh et al., p. 68, ESSCIRC2007

Breakthrough Technologies

for reducing V_{min} and V_{ps}

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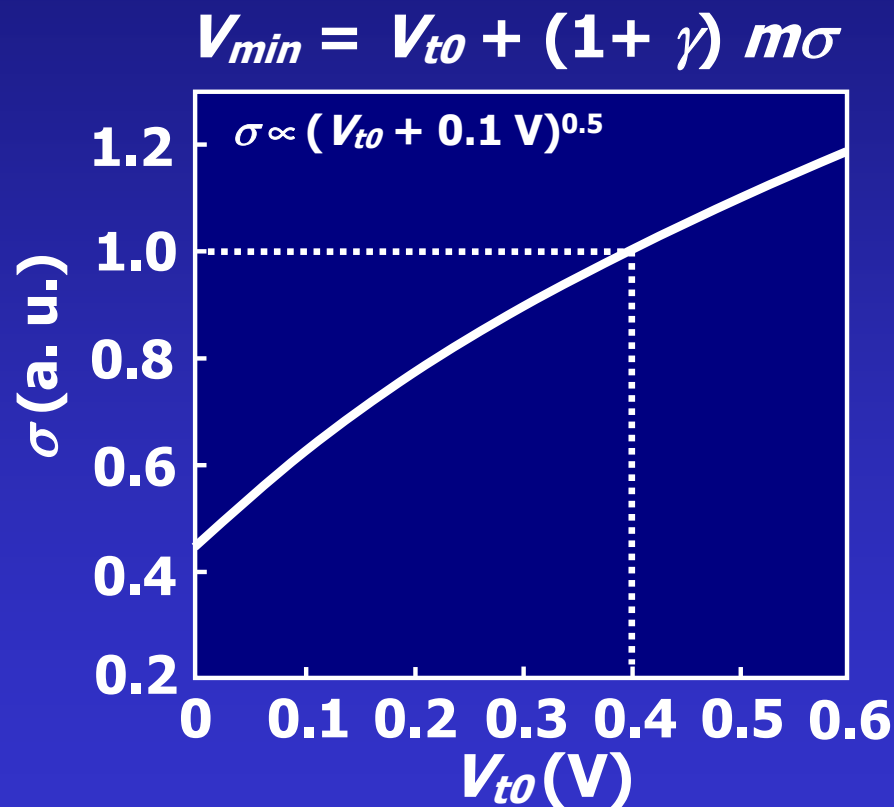
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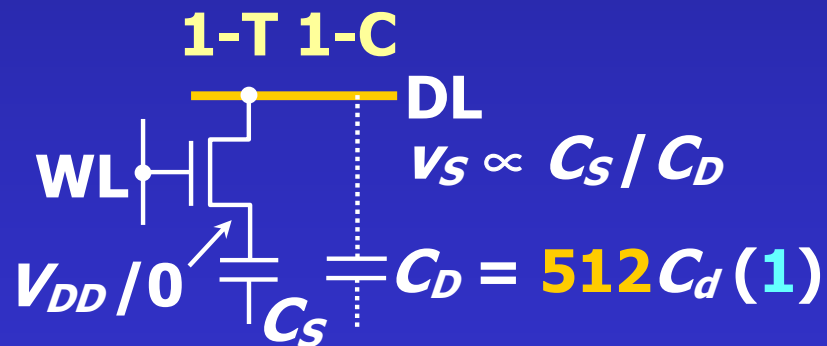
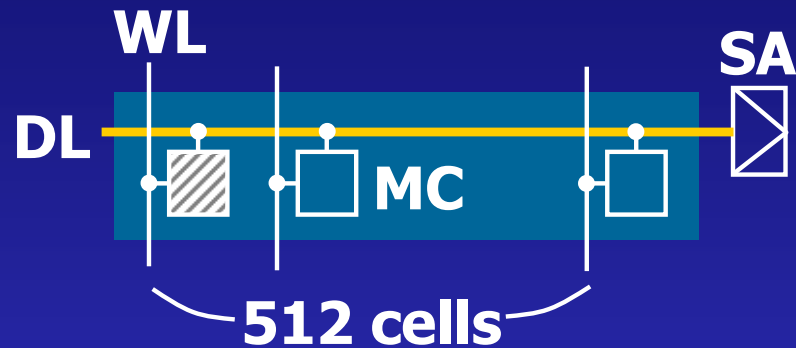
- 2-D selection FinFET cell
- Many-core and chip stack



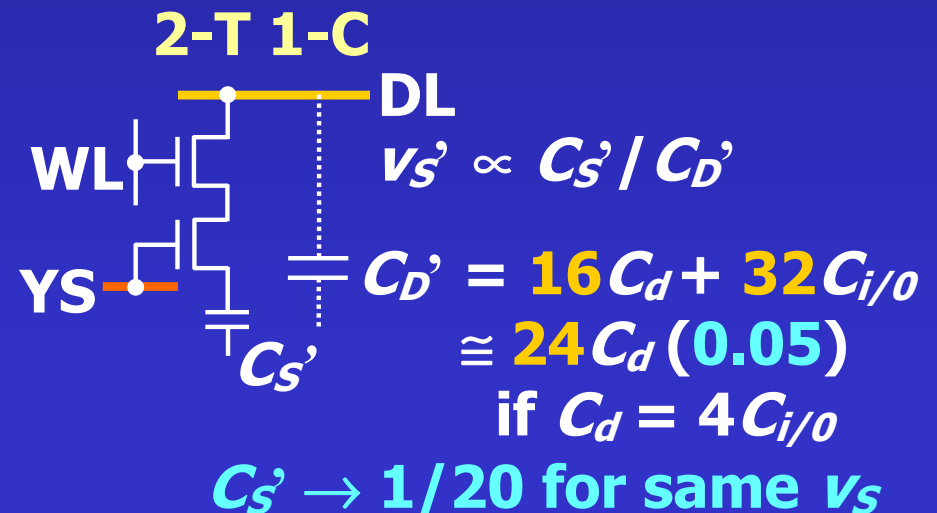
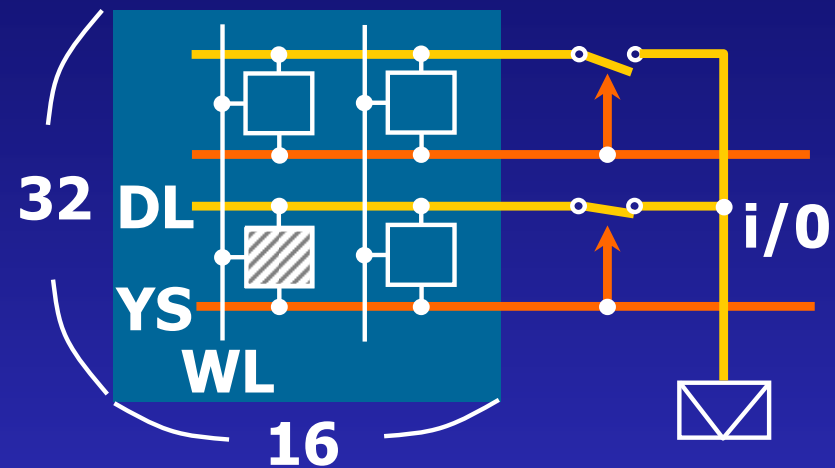
Future Perspectives, ISLPED'02, August 2002.

2-D Selection DRAM Cell

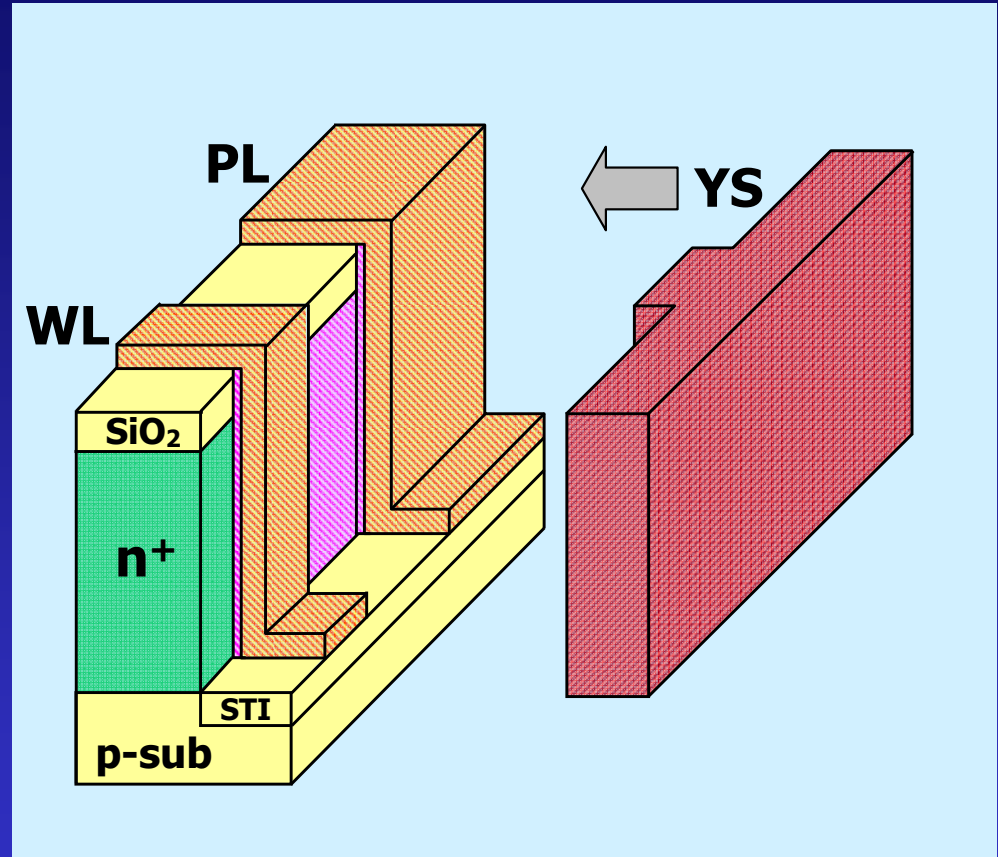
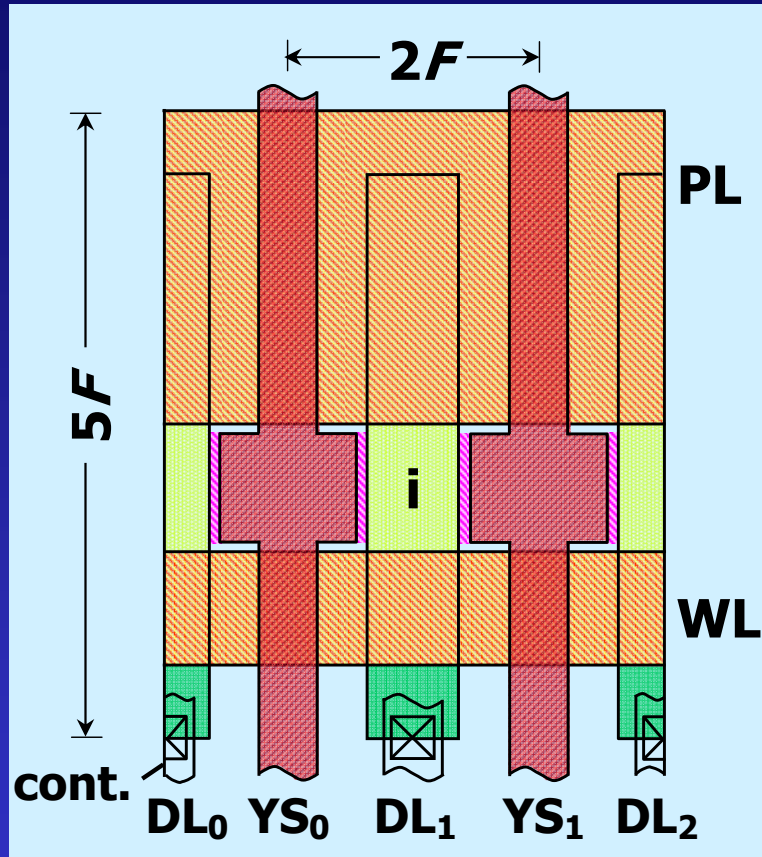
Conventional



2-D selection



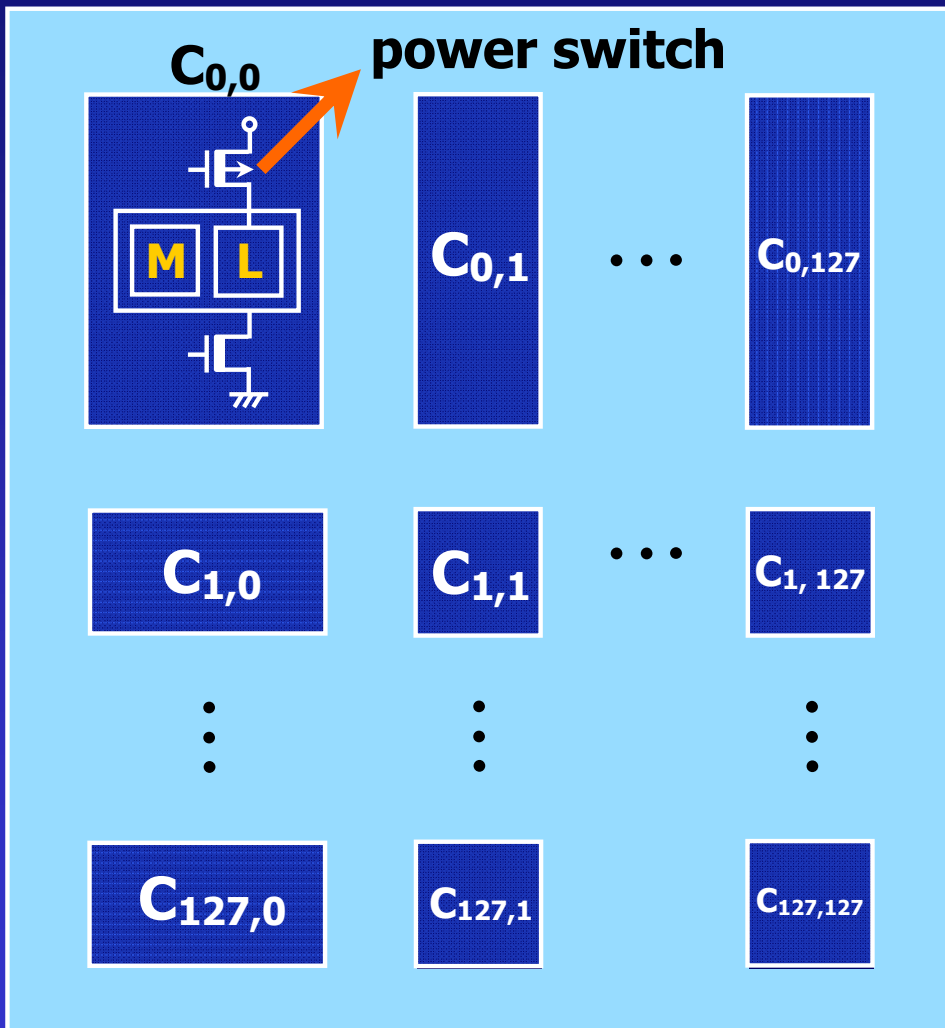
2-T FinFET DRAM Cell



- A FinFET and FinFET capacitor at the side wall
 - Another FinFET with the gate controlled by buried YS line
 - One DL shared by two cells
- $5F^2/\text{cell}$ (cf. $6-8F^2$ for DRAMs, $>160F^2$ for SRAMs)

Many-Core LSI

16k cores in the 11-nm generation



Chip: 10 x 10 mm²

320 Mg, 8-Gb DRAM

Small Core: 56 x 56 μm²

20-Kg + others (0.67)

512-Kb DRAM (0.33)

5F² cell

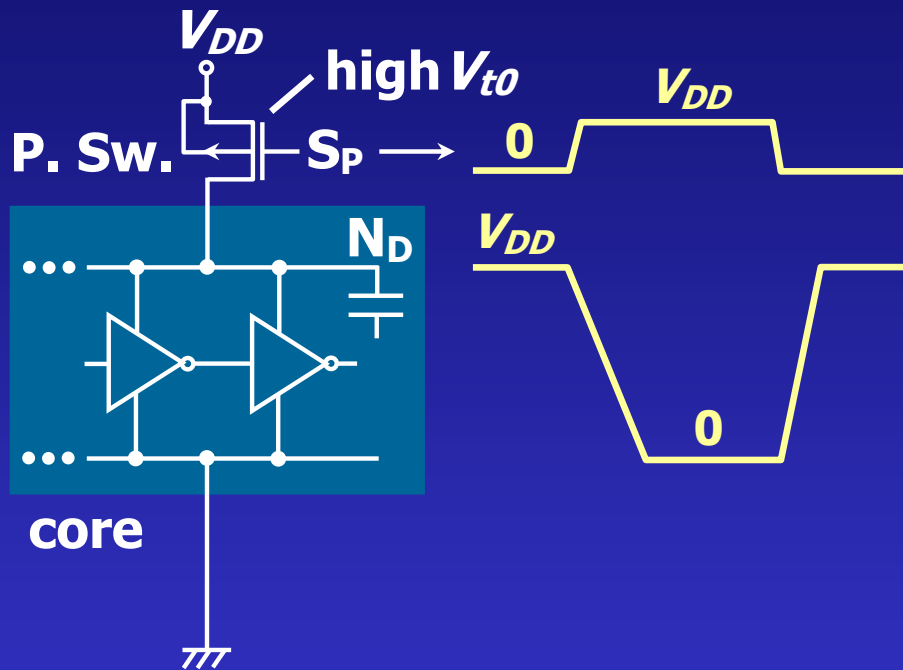
Challenges:

Develop

- Redundant circuits/cores
- LN HS power switch etc.

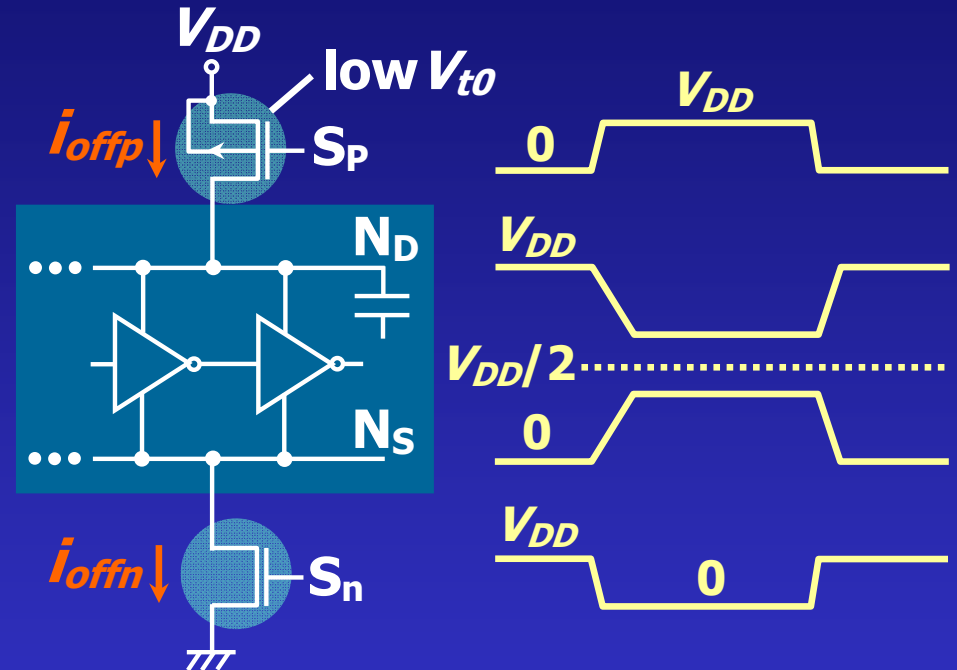
Differentially-Driven Low- V_{t0} Power Switches

Conventional



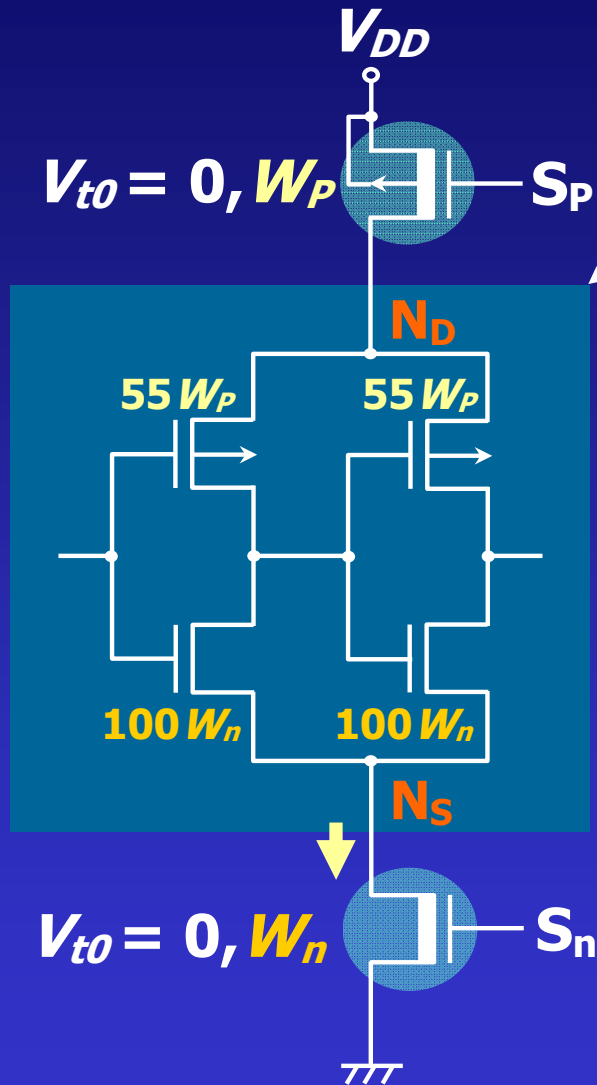
- Large V_{PS} (V_{DD} swing of N_D)
- Int. logic state destroyed
- Slow recovery of N_D

Proposed

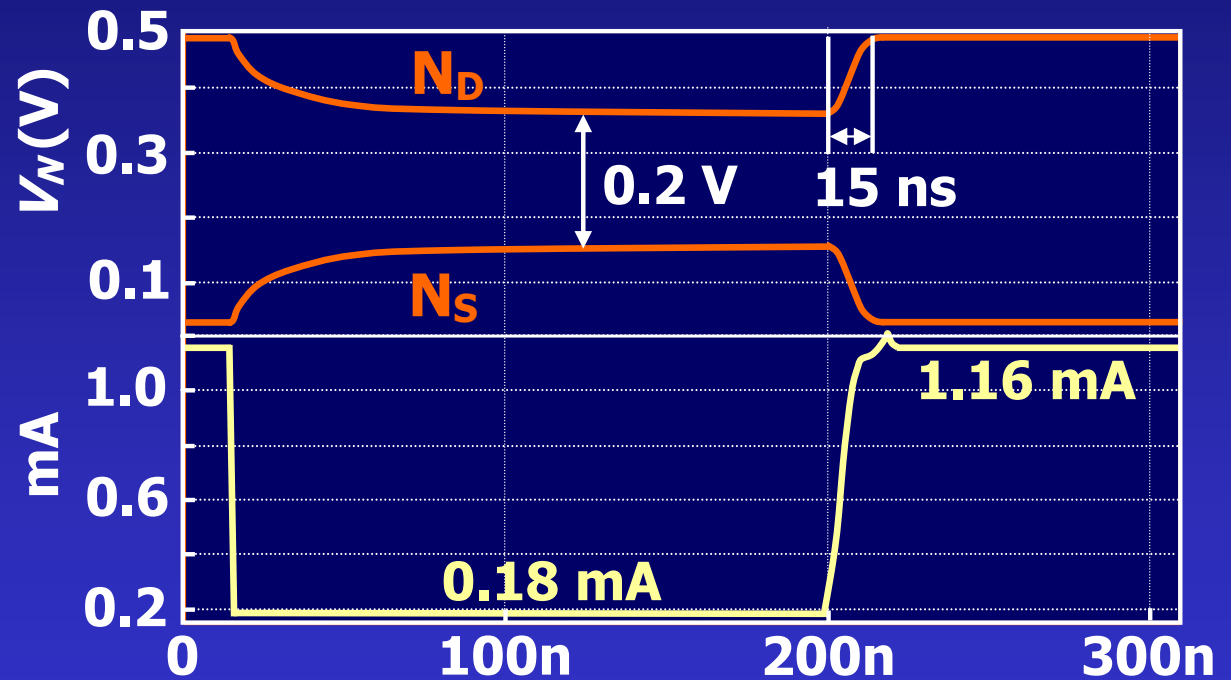


- If $i_{offp} = i_{offn}$, N_D & $N_S \rightarrow V_{DD}/2$.
- V_{PS} canceled.
(differentially-driven N_D & N_S)
 - Int. logic state held
 - Fast recovery

Simulation Results



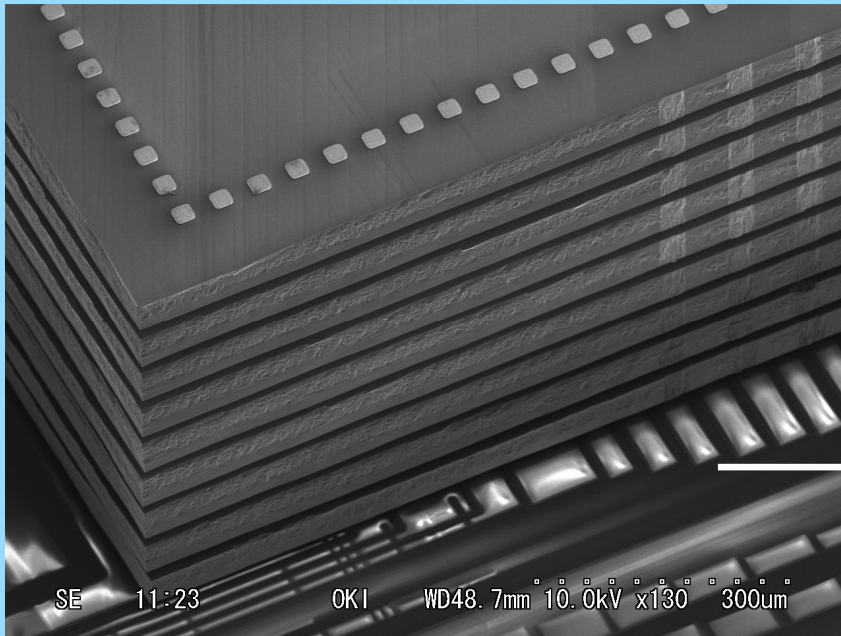
20-kgate core
 $V_{DD} = 0.5 \text{ V}, V_{t0} = 0.2 \text{ V}, 85^\circ\text{C}$



Leakage power of 16k cores:
1.4 W (standby)
9.3 W (active, all cores activated)

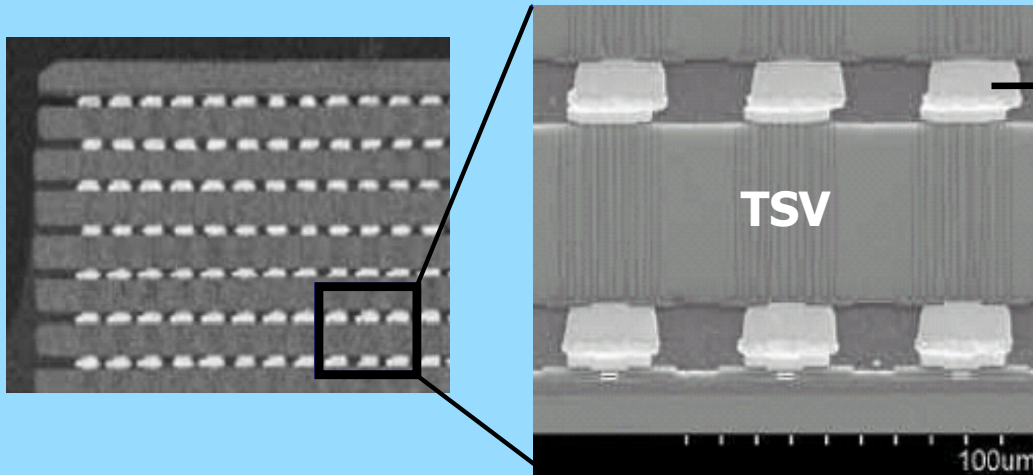
$W_P = 320 \times 360 \text{ nm}$
 $W_n = 240 \times 190 \text{ nm}$
 $L = 50 \text{ nm}$

Chip Stack



9 stacked DRAM chips
(each **50 μ m** thick)

Interface chip

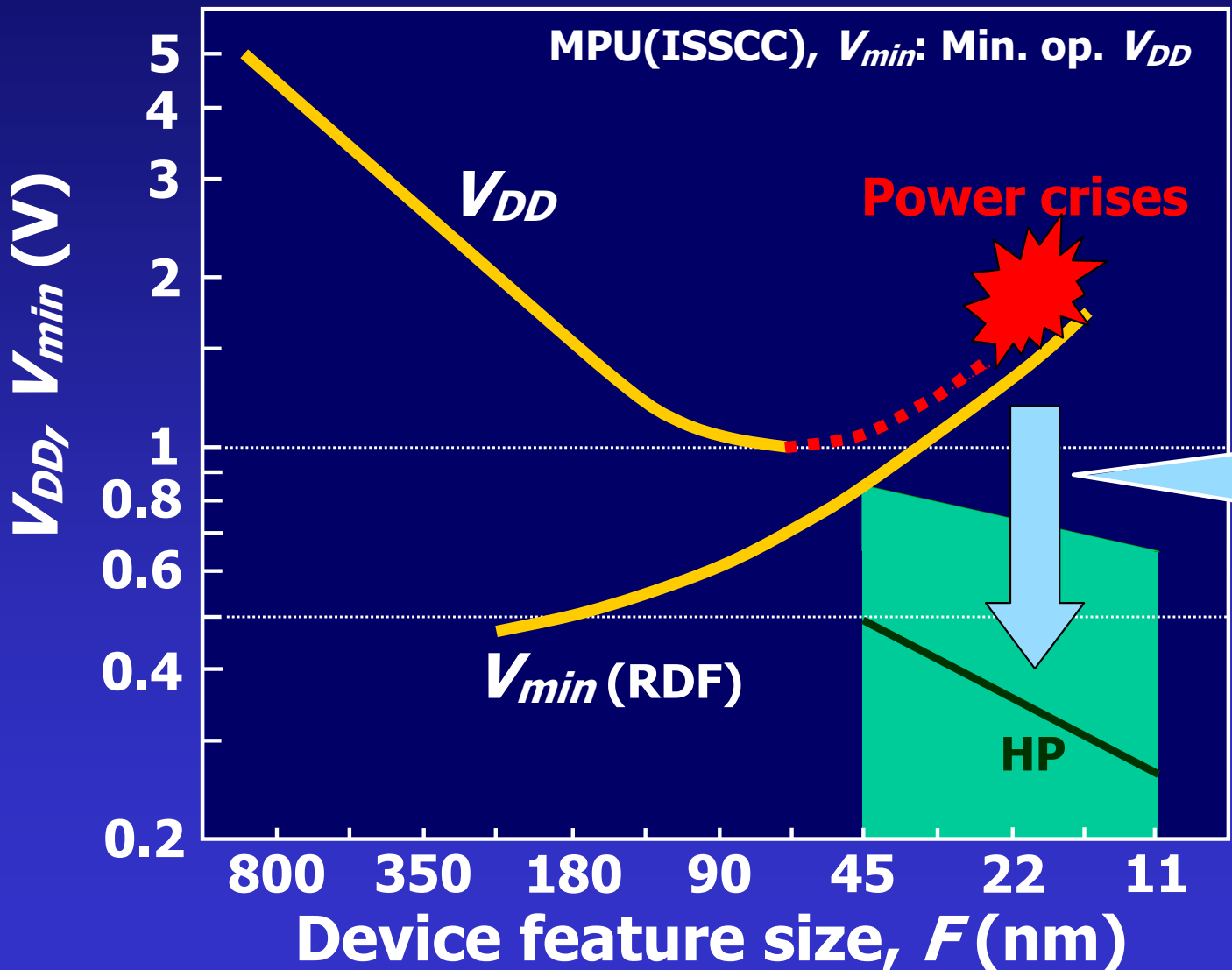


Bump

TSV: Through
Silicon Via

by courtesy of ELPIDA

Scenario to the 0.5-V Era



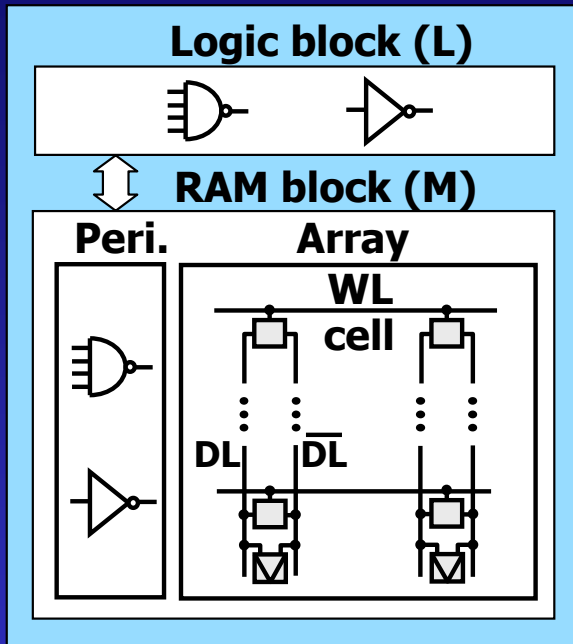
Breakthrough

- Repair
- σ -scalable MOS (FinFET)
- Dual- V_{DD} dual- V_{t0} circuits
- Tiny DRAM cell
- Many-core LSIs
- LN HS power gating

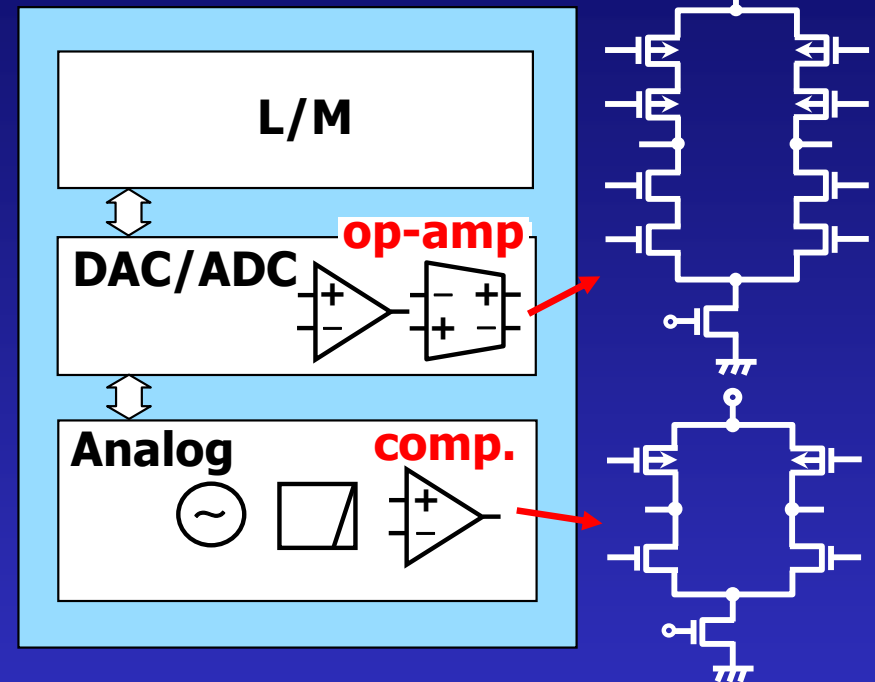
RDF: Random Dopant Fluctuation

Memory-Rich LSI vs. Mixed Signal LSI

Memory-rich LSI



Mixed signal LSI

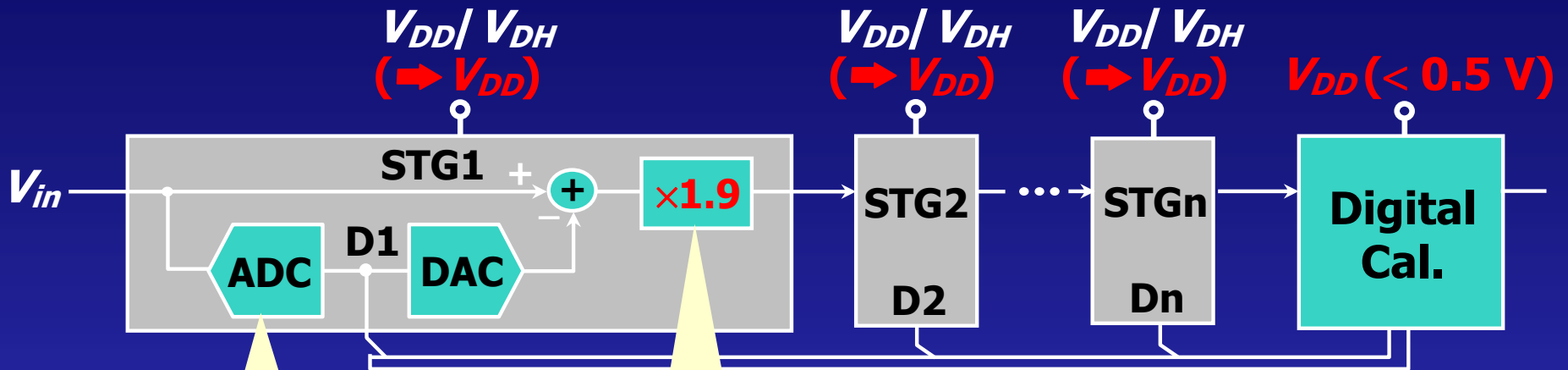


	Inv.	SRAM cell	DRAM SA
Count*	640M	2G	128M
LW	$8F^2$	$1.5F^2$	$15F^2$
ΔV_{tmax}^*	27 mV	34 mV	10 mV

	Cascode amp	Diff. amp
Count*	20	200
LW	$3000F^2$	$300F^2$
ΔV_{tmax}^*	0.5 mV	2.3 mV

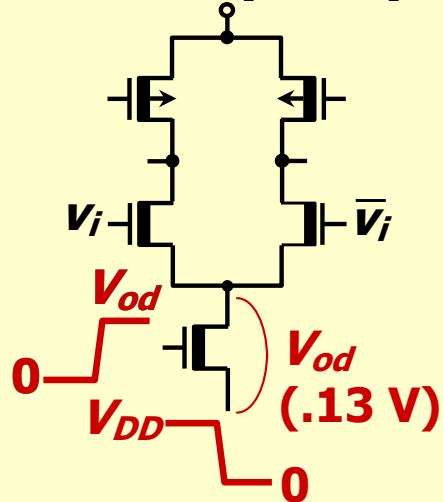
* $A_{vt} = 1.25 \text{ mV}\mu\text{m}$, $V_{t0} = 0$, 11-nm FinFET, repair for RAMs

Digital Assisted Analog Design-Pipeline ADC



comp.

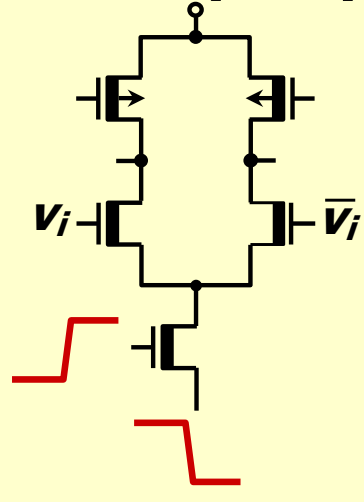
$V_{DD} (> V_{min})$



$$V_{min} \cong 3 V_{od} \cong 0.4 \text{ V}$$

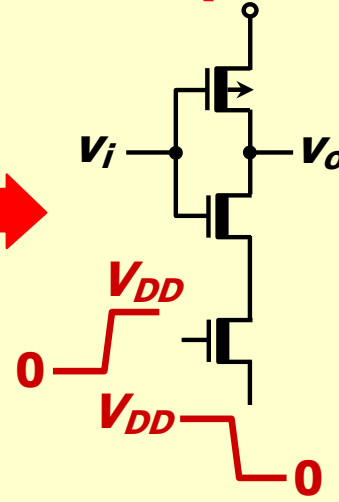
op-amp

$V_{DH} (> V_{DD})$



$$V_{min} \cong 3 V_{od} + V_{dyn} \cong 0.9-0.7 \text{ V}$$

$V_{DD} (> V_{min})$



$$V_{min} \cong V_{dyn} (< 0.5 \text{ V})$$

- Lower- V_{to} MOS

Better signal integrity

- FinFET

Small $\Delta V_{Tmax} / V_{off}$

No body effect

Small sub. noise

High-density C

(large LW)

High-Q inductor

Conclusion

- **The 1-V wall breached with adaptive circuits.**
- **The 0.5-V nanoscale era will open the door to lower power dissipation, if relevant devices and fabrication processes are developed.**
- **Disruptive inventions and technologies, which some of you may come up with, will make such an era an even closer reality.**

For additional multimedia material: See <http://www.isscc.org>

