Adaptive Circuits
for
the 0.5-V Nanoscale CMOS Era

Kiyoo Itoh
Hitachi Ltd., Tokyo, Japan
OUTLINE

1. Introduction
   The 1-V wall

2. Adaptive Circuits for Memory-Rich LSIs
   Trends in $V_{\text{min}}$
   Breakthrough technologies
   Scenario to the 0.5-V nanoscale era

3. Adaptive Circuits for Mixed Signal LSIs
   Digital assisted analog design

4. Conclusion
The 1-V Wall

$V_{DD}$, $V_{min}$ (RDF)

Target

MPUs (ISSCC), $V_{min}$: Min. op. $V_{DD}$

Power crisis

Device feature size, $F$ (nm)

RDF: Random Dopant Fluctuation

$V_{DD}$

$V_{min}$ (RDF)
What should we do to lower $V_{DD}$?

1. Reduce min. operating $V_{DD}$ ($V_{min}$) by reducing:
   - Lowest necessary $V_t$ ($V_{t0}$),
   - Intrinsic $V_t$-variation ($\Delta V_t$).
   → New devices, circuits, repair etc.

2. Reduce power-supply noise ($V_{ps}$)
   → Compact subsystems (small core/chip, 3-D chip stack) etc.

Reducing $V_{min}$ is the key. ($V_{min} \gg V_{ps}$)
OUTLINE

1. Introduction
   The 1-V wall

2. Adaptive Circuits for Memory-Rich LSIs
   Trends in $V_{\text{min}}$
   Breakthrough technologies
   Scenario to the 0.5-V nanoscale era

3. Adaptive Circuits for Mixed Signal LSIs
   Digital assisted analog design

4. Conclusion
Circuits Giving Low-$V_{DD}$ Limitations

* Most sensitive to $\Delta V_t$

$\Delta V_t \propto 1/\sqrt{LW}$, $F$: device feature size

<table>
<thead>
<tr>
<th>Chip</th>
<th>Logic block</th>
<th>RAM block</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>SRAM Cell*</td>
<td>DRAM SA*</td>
</tr>
<tr>
<td>Count</td>
<td>large</td>
<td>largest</td>
</tr>
<tr>
<td>$LW$</td>
<td>8$F^2$(av.)</td>
<td>1.5-3$F^2$</td>
</tr>
<tr>
<td>$\Delta V_t$</td>
<td>large</td>
<td>largest</td>
</tr>
</tbody>
</table>
Definition of $V_{\text{min}}$

$\tau(V_t) \propto V_{DD}/(V_{DD} - V_t)^{1.2}$

$\Delta \tau = \tau(V_{t0} + \Delta V_{t\text{max}})/\tau(V_{t0})$

$= \left\{(V_{DD} - V_{t0})/(V_{DD} - V_{t0} - \Delta V_{t\text{max}})\right\}^{1.2}$

$V_{t0}$: Lowest necessary avg. $V_t$

$\Delta V_{t\text{max}}$: Max. variation in $V_t$

$V_{\text{min}} = V_{DD}$ for a fixed $\Delta \tau$

$= V_{t0} + (1 + \gamma) \Delta V_{t\text{max}}$

$\gamma = 1/(\Delta \tau^{1/1.2} - 1)$

$\Delta \tau$: Tolerable speed variation

$\gamma \approx 2–3$ for $\Delta \tau = 1.4 – 1.6$
High and Unscalable $V_{to}$

HP: high performance, LP: low power

$V_{to}(\text{ext}) = V_{to}(\text{nA/\mu m}) + 0.3 \text{ V}$

$T_j = 75^\circ \text{C}, 130 \text{ nm}$

*$\text{contributing to leakage in active standby mode}$

K. Itoh

© 2009 IEEE International Solid-State Circuits Conference

© 2009 IEEE
$\Delta V_{t_{\text{max}}} = m \sigma$

- $m \to$ circuit count
- $\sigma = \frac{A_{vt}}{\sqrt{LW}}$
  $\propto \{t_{\text{ox}}(V_{t0} + 0.1 \text{ V})\}^{0.5}$
  $\propto N_{\text{sub}}^{0.25}$

For lower $\Delta V_{t_{\text{max}}}$, use

1. Repair
   - ECC + Redundancy ($m \to 1/2$)
2. Small $\sigma$ technologies
   - Circuits tolerating
     The largest MOSFET possible
     The lowest $V_{t0}$ possible
   - Small-$A_{vt}$ MOSFETs

K. Itoh et al., p. 68, ESSCIRC2007
K. Takeuchi et al., p. 467, IEDM 2007
ECC + Redundancy

- ECC word with one defect cell corrected by ECC.
- ECC word with two or more defects replaced by a redundant word.

$W$ ECC Words

Redundant Words

Parity bits

Data bits

Defective cell replace

$r$: repairable %
Max $r = 0.1\%$(SRAMs), 0.4\%$(DRAMs).

K. Itoh, ESSCIRC2007 Dig., pp. 68-75

© 2009 IEEE International Solid-State Circuits Conference

© 2009 IEEE
Trends in $V_{min}$

$$\sigma = \frac{A_{vt}}{\sqrt{LW}}$$

$LW = 8F^2(L), 1.5F^2(SRAM), 15F^2(DRAM)$

$A_{vt} = 4.2 \text{ mV}\mu\text{m (Conv.)}$

$A_{vt} = 1.5 \text{ mV}\mu\text{m (Hi-k MG, SOI)}$

$V_{t0} = 0.4 \text{ V}$

$V_{min} (V)$

$F (\text{nm})$ 250 180 130 90 65 45 32 22 15 11

Logic (g) 1.3M 5M 20M 80M 320M

SRAM (b) 8M 32M 128M 512M 2G

DRAM (b) 32M 128M 512M 2G 8G

Repair for RAMs
State-of-the-Art SRAM Cells

Increased cell-power supply

Dynamic S-control

Dynamic S-control

8-T cell

Reduction in $V_{\text{min}}$ of SRAMs

6-T cell

$\Delta \tau = 1.6$, repair
$A_{\text{vt}} = 2.5 \text{ mV} \mu \text{m}$

$V_{\text{to}} = 0.4 \text{ V}$

$LW \propto F^2$

Cell size (ratio)

Device feature size, $F (\text{nm})$

6-T cell vs 8-T cell

$LW \propto F^2$

8-T, $LW \propto F^2$

$W$ fixed at 90 nm

$156-185 F^2$

$120 F^2$

$W$ fixed at 90 nm

$V_{\text{min}} (V)$

$F (\text{nm})$

$0.2$ $0.3$ $0.4$ $0.5$ $0.6$ $0.7$ $0.8$ $0.9$ $1.0$ $1.1$

$0.2$ $0.4$ $0.6$ $0.8$ $1.0$

$250$ $130$ $65$ $32$ $15$

SRAM(b) $4 \text{ M}$ $16 \text{ M}$ $64 \text{ M}$ $256 \text{ M}$ $1 \text{ G}$

$\Delta \tau = 1.6$, repair
$A_{\text{vt}} = 2.5 \text{ mV} \mu \text{m}$

$V_{\text{to}} = 0.4 \text{ V}$

$LW \propto F^2$

Cell size (ratio)

Device feature size, $F (\text{nm})$

6-T

8-T, $LW \propto F^2$

$156-185 F^2$

$120 F^2$

$W$ fixed at 90 nm

$V_{\text{min}} (V)$

$F (\text{nm})$

$0.2$ $0.3$ $0.4$ $0.5$ $0.6$ $0.7$ $0.8$ $0.9$ $1.0$ $1.1$

$0.2$ $0.4$ $0.6$ $0.8$ $1.0$

$250$ $130$ $65$ $32$ $15$

SRAM(b) $4 \text{ M}$ $16 \text{ M}$ $64 \text{ M}$ $256 \text{ M}$ $1 \text{ G}$
1. Adaptive devices/circuits
   ($V_{min} \downarrow$)
   - $\sigma$-scalable FinFET
   - Dual-$V_{DD}$ dual-$V_{t0}$ circuit

2. Adaptive tech. ($V_{ps} \downarrow$)
   with small chip/compact subsystem
   - 2-D selection FinFET cell
   - Many-core and chip stack
Assumptions for $A_{vt}$ and $V_{t0}$

$$\sigma = \frac{A_{vt}}{\sqrt{LW}}, \quad \alpha > 1 \quad (\alpha: \text{device scaling factor})$$

$A_{vt} \propto \frac{1}{\sqrt{\alpha}}$

$V_{t0} = 0.4 \text{ V}$

$A_{vt} \propto \frac{1}{\alpha}$

$V_{t0} = 0.2 \text{ V}$
$\sigma$-Scalable FinFET
by scaling up the height of fin

<table>
<thead>
<tr>
<th></th>
<th>Planar</th>
<th>FinFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\sigma$</td>
<td>$1$</td>
<td>$1/\alpha$</td>
</tr>
<tr>
<td>$A_{vt}$</td>
<td>$1/\alpha$</td>
<td>$1/\alpha$</td>
</tr>
<tr>
<td>$L$</td>
<td>$1/\alpha$</td>
<td>$1/\alpha$</td>
</tr>
<tr>
<td>$W$</td>
<td>$1/\alpha$</td>
<td>$1/\alpha$</td>
</tr>
<tr>
<td>$LW$</td>
<td>$1/\alpha^2$</td>
<td>$1/\alpha^2$</td>
</tr>
</tbody>
</table>

$\alpha > 1$, $\sigma = A_{vt}/\sqrt{LW}$
$\sigma$ and $V_{min}$ for HP Designs

- **Device feature size, $F$ (nm)**: 45, 32, 22, 15, 11

  - **SRAM**
  - **Logic**
  - **DRAM**

- **$\sigma$ (mV)**: 50, 40, 30, 20, 10, 5, 4, 3, 2

- **$V_{min}$ (V)**: 1, 0.5, 0.4, 0.3, 0.2, 0.1

- **Repair for RAMs**
  - **Logic (g)**
  - **SRAM (b)**
  - **DRAM (b)**

- **Logic (g)**: 20M, 40M, 80M, 160M, 320M

- **SRAM (b)**: 128M, 256M, 512M, 1G, 2G

- **DRAM (b)**: 512M, 1G, 2G, 4G, 8G

© 2009 IEEE International Solid-State Circuits Conference
σ and $V_{min}$ for LP Designs

- **σ (mV)**
  - SRAM
  - Logic
  - DRAM

- **$V_{min}$ (V)**
  - SRAM
  - Logic
  - DRAM

**Device feature size, $F$ (nm)**
- 45
- 32
- 22
- 15
- 11

**Repair for RAMs**
- Logic
- SRAM

- Logic
- SRAM

- 1.4
- 1.3
- 0.65

© 2009 IEEE International Solid-State Circuits Conference
Dual- $V_{DD}$ Dual- $V_{t0}$ Dynamic Circuit

$V_{min}$ for dual- $V_{DD}$ dual- $V_{t0}$ circuit

$V_{t0} = 0.4 \text{ V}$

$V_{t0} = 0 \text{ V}$

Device feature size, $F$ (nm)

0.65

0.11

Logic block

$V_{DD}$, $V_{tH}$

$V_{DL}$, $V_{tL}$

Bigger area of $V_{DL}$ sub-block → Lower $V_{min}$
Gate-Source Offset Driving

\[ V_{teff} = \Delta V + V_t \geq V_{t0} \]

\[ V_G = V_{DL} - V_t \]

\[ V_{DD} = 0.6 \, \text{V} \]
\[ V_{teff} = V_{t0} = 0.3 \, \text{V} \]
\[ V_G = 0.3 \, \text{V} \]

K. Itoh et al., p. 68, ESSCIRC2007
0.1-V Swing E/D Dynamic Inverter

$V_{DL} = 0.1 \text{ V, } V_{DD} = 0.6 \text{ V}$

D-MOS ($V_t = 0.2 \text{ V}$)

Widely applicable to low-power buffers and others.

Others: E-MOS ($V_t = 0.3 \text{ V}$). $W(\text{nm})=140(M_1,M_3)$, $420(M_2)$, $280(M_4)$, $L=50 \text{ nm}$ $C_L = 4\text{fF}+4\text{MOSs}$. 

K. Itoh et al., p. 68, ESSCIRC2007
Breakthrough Technologies

for reducing $V_{min}$ and $V_{ps}$

The best way to predict the future is to invent it.

1. Adaptive devices/circuits ($V_{min}$ ↓)
   - $\sigma$-scalable FinFET
   - Dual-$V_{DD}$ dual-$V_{to}$ circuit

2. Adaptive tech. ($V_{ps}$ ↓)
   with small chip/compact subsystem
   - 2-D selection FinFET cell
   - Many-core and chip stack

Future Perspectives, ISLPED’02, August 2002.
2-D Selection DRAM Cell

Conventional

1-T 1-C

\[ V_{DD} / 0 \]

\[ C_d = 512C_d \]

\[ V_S \propto C_S / C_D \]

\[ C_D = 512C_d \]

2-D selection

2-T 1-C

\[ C_S' \rightarrow 1/20 \text{ for same } V_S \]

\[ C_d = 4C_{i/0} \]

\[ C_d = 16C_d + 32C_{i/0} \]

\[ C_d \approx 24C_d (0.05) \]

\[ C_S' = 16C_d + 32C_{i/0} \]

\[ C_d = 4C_{i/0} \]
2-T FinFET DRAM Cell

- A FinFET and FinFET capacitor at the side wall
- Another FinFET with the gate controlled by buried YS line
- One DL shared by two cells
  → $5F^2$/cell (cf. $6-8F^2$ for DRAMs, $>160F^2$ for SRAMs)
Many-Core LSI

16k cores in the 11-nm generation

Chip: 10 x 10 mm²
320 Mg, 8-Gb DRAM

Small Core: 56 x 56 μm²
20-Kg + others (0.67)
512-Kb DRAM (0.33)
5F² cell

Challenges:
Develop
• Redundant circuits/cores
• LN HS power switch etc.
Differentially-Driven Low-\( V_{t0} \) Power Switches

**Conventional**

- Large \( V_{PS} \) (\( V_{DD} \) swing of \( N_D \))
- Int. logic state destroyed
- Slow recovery of \( N_D \)

**Proposed**

- \( V_{PS} \) canceled.
- (differentially-driven \( N_D \) & \( N_S \))
- Int. logic state held
- Fast recovery

If \( i_{offp} = i_{offn} \), \( N_D \) & \( N_S \) $\rightarrow V_{DD}/2$. 

\( V_{DD} / 2 \)
Simulation Results

20-kgate core

$V_{DD} = 0.5$ V, $V_{t0} = 0.2$ V, 85°C

$V_{t0} = 0, W_P$

$W_P = 320 \times 360$ nm

$W_n = 240 \times 190$ nm

$L = 50$ nm

Leakage power of 16k cores:

1.4 W (standby)

9.3 W (active, all cores activated)
Chip Stack

9 stacked DRAM chips (each $50\mu m$ thick)

Interface chip

Bump

TSV: Through Silicon Via

by courtesy of ELPIDA
Scenario to the 0.5-V Era

MPU(ISSCC), $V_{\text{min}}$: Min. op. $V_{\text{DD}}$

- Repair
- $\sigma$-scalable MOS (FinFET)
- Dual-$V_{\text{DD}}$ dual-$V_{t0}$ circuits
- Tiny DRAM cell
- Many-core LSIs
- LN HS power gating

Device feature size, $F$ (nm)

RDF: Random Dopant Fluctuation

$V_{\text{DD}}$, $V_{\text{min}}$ (V)
Memory-Rich LSI vs. Mixed Signal LSI

Memory-rich LSI

Logic block (L)

RAM block (M)

Peri. Array

WL cell

DL

DL

Mixed signal LSI

L/M

DAC/ADC

op-amp

Analog comp.

<table>
<thead>
<tr>
<th>Inv.</th>
<th>SRAM cell</th>
<th>DRAM SA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Count*</td>
<td>640M</td>
<td>2G</td>
</tr>
<tr>
<td>LW</td>
<td>$8F^2$</td>
<td>$1.5F^2$</td>
</tr>
<tr>
<td>$\Delta V_{tmax}^*$</td>
<td>27 mV</td>
<td>34 mV</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Cascode amp</th>
<th>Diff. amp</th>
</tr>
</thead>
<tbody>
<tr>
<td>Count*</td>
<td>20</td>
</tr>
<tr>
<td>LW</td>
<td>$3000F^2$</td>
</tr>
<tr>
<td>$\Delta V_{tmax}^*$</td>
<td>0.5 mV</td>
</tr>
</tbody>
</table>

*$A_{vt} = 1.25 \text{ mV}\mu\text{m}, V_{to} = 0, 11$-nm FinFET, repair for RAMs

K. Itoh

© 2009 IEEE International Solid-State Circuits Conference
Digital Assisted Analog Design-Pipeline ADC

- Lower $V_{t0}$ MOS
  - Better signal integrity
- FinFET
  - Small $\Delta V_{T_{max}}/V_{off}$
  - No body effect
  - Small sub. noise
  - High-density C (large $LW$)
  - High-Q inductor

$V_{DD}/V_{DH}$ ($\leftrightarrow V_{DD}$)

$V_{DD}(<0.5 \text{ V})$

$V_{in}$

ADC

DAC

comp.

$V_{DD}(>V_{min})$

$V_{min} \equiv 3V_{od} \cong 0.4 \text{ V}$

$V_{od}(0.13 \text{ V})$

op-amp

$V_{DH}(>V_{DD})$

$V_{min} \equiv 3V_{od} + V_{dyn} \cong 0.9-0.7 \text{ V}$

$V_{min} \equiv V_{dyn} (<0.5 \text{ V})$

$V_{DD}$

$V_{DH}$
Conclusion

- The 1-V wall breached with adaptive circuits.
- The 0.5-V nanoscale era will open the door to lower power dissipation, if relevant devices and fabrication processes are developed.
- Disruptive inventions and technologies, which some of you may come up with, will make such an era an even closer reality.
For additional multimedia material: See http://www.isscc.org