

# Energy Efficient Circuit Design and the Future of Power Delivery

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# Outline

- **Looking back**
- **Energy efficiency in CMOS**
- **Side effects**
- **Suggestions**
- **Conclusion**



# Looking Back

- **Microprocessor scaling has been a topic of interest both at EPEP and to the IC design community in general**
  - **MOS scaling helps set our expectations for the future**
  - **Microprocessors tend to bound the high power density edge of the product space**



# EPEP 2003

- In his “Architecting Interconnect” address, Peter Hofstee identified the major challenges facing microprocessors:
  - Software inertia
  - I/O bandwidth
  - Power delivery
  - Cooling
- The future is simpler architecture and more cores

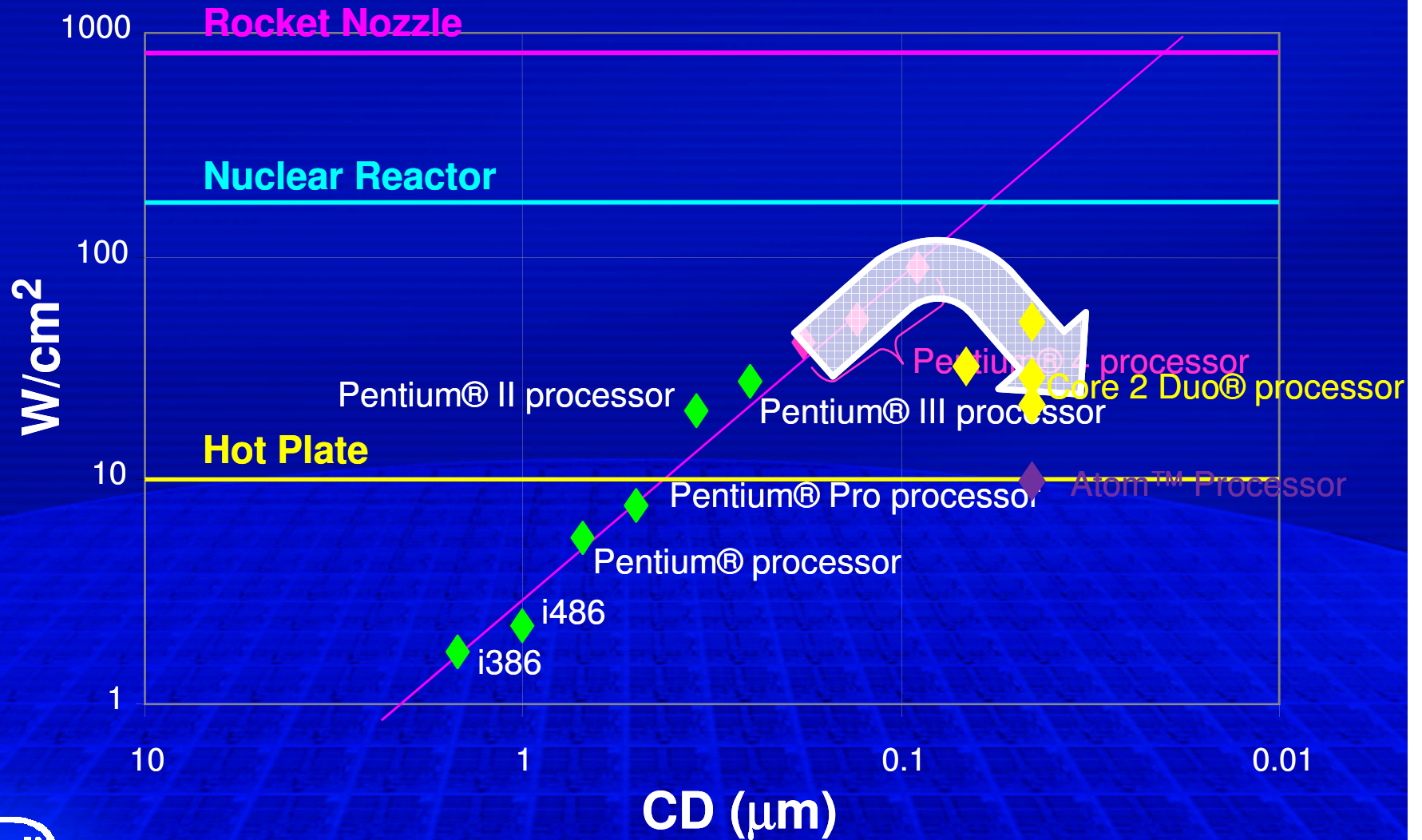


# SPI 2004

- In my “Design Challenges of the 90 nm Pentium® 4 Processor” address highlighted similar issues:
  - Power delivery
  - Cooling
  - Variation
  - Gate leakage
- But scaling will continue



# Power density vs CD

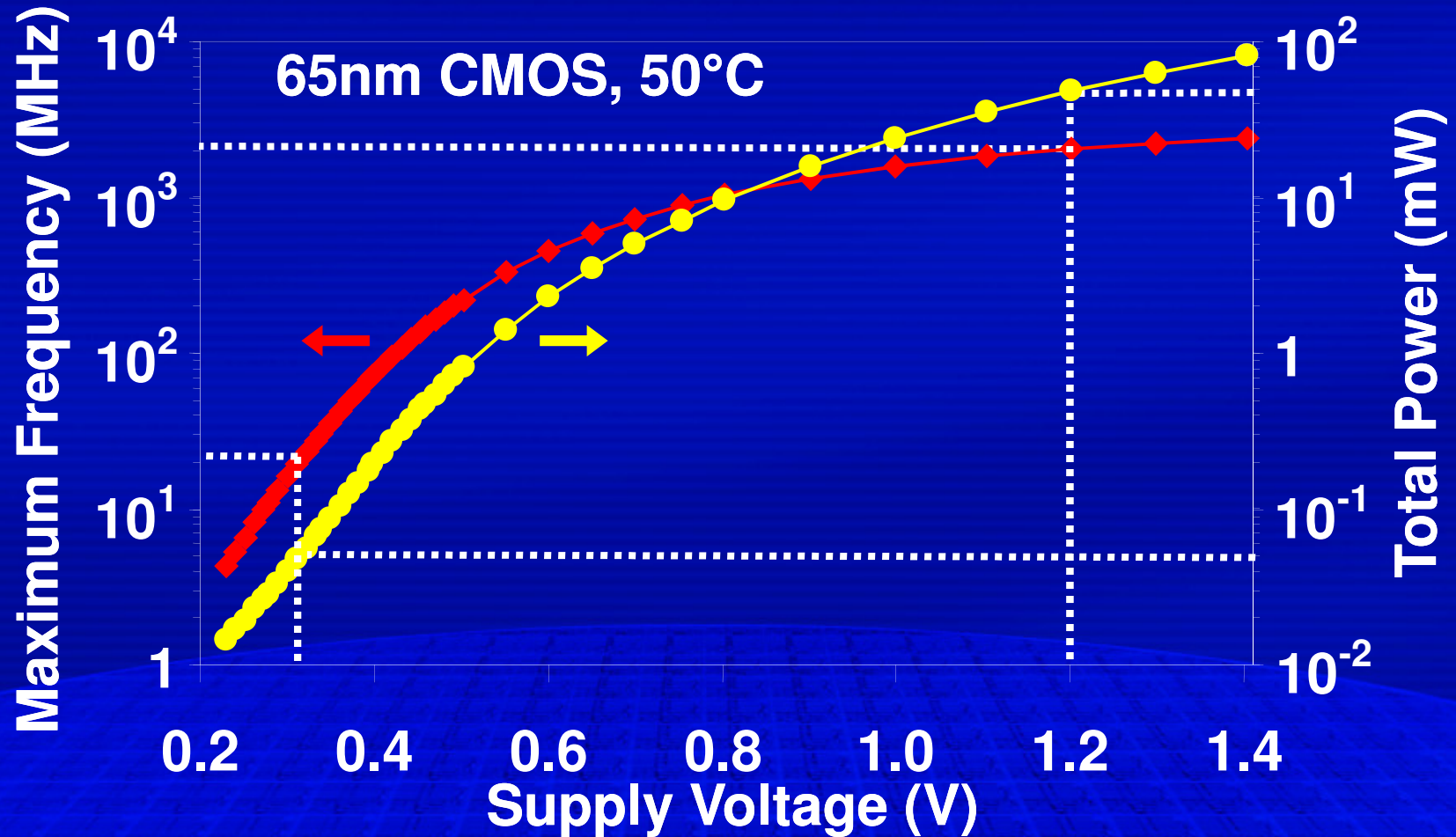


# Energy Efficiency in CMOS

- CMOS power is determined by C, V, f:
  - Power  $\sim CV^2f + I_{\text{leak}}V$
- Process technology can improve C
- Reducing V reduces performance
  - Delay  $\sim C * V_{\text{cc}} / (V_{\text{cc}} - V_{\text{t}})^{\alpha}$
- But it reduces power even faster
  - $I_{\text{leak}}$  is also a function of V



# Frequency and Power Measurements

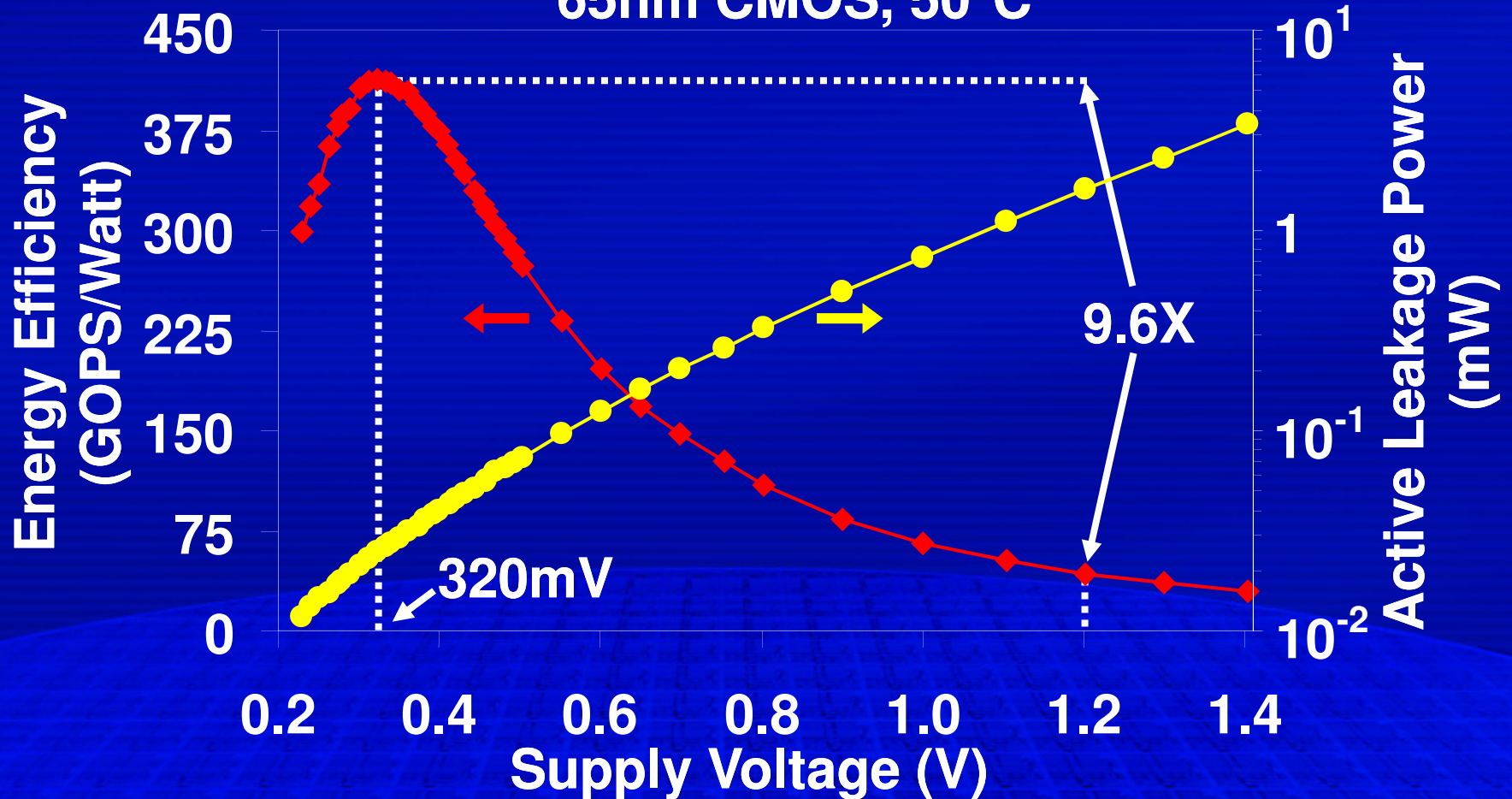


- From: A 320mV 56 $\mu$ W 411GOPS/Watt Ultra-Low Voltage Motion Estimation Accelerator in 65nm CMOS – ISSCC '08



# Energy-Efficiency Measurements

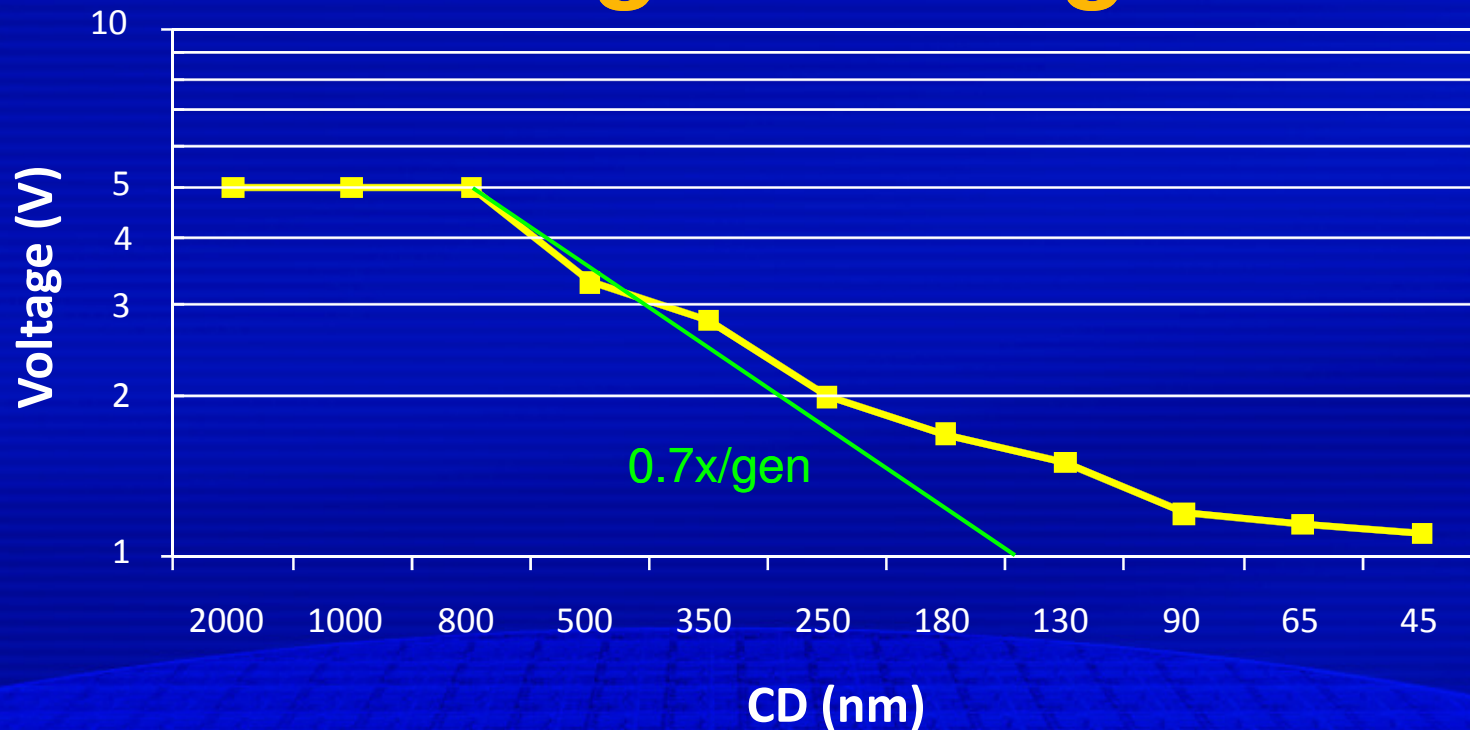
65nm CMOS, 50°C



- From: A 320mV 56 $\mu$ W 411GOPS/Watt Ultra-Low Voltage Motion Estimation Accelerator in 65nm CMOS – ISSCC '08



# Voltage Scaling



- Voltage scaling has slowed on recent technologies
  - This is the technology maximum voltage

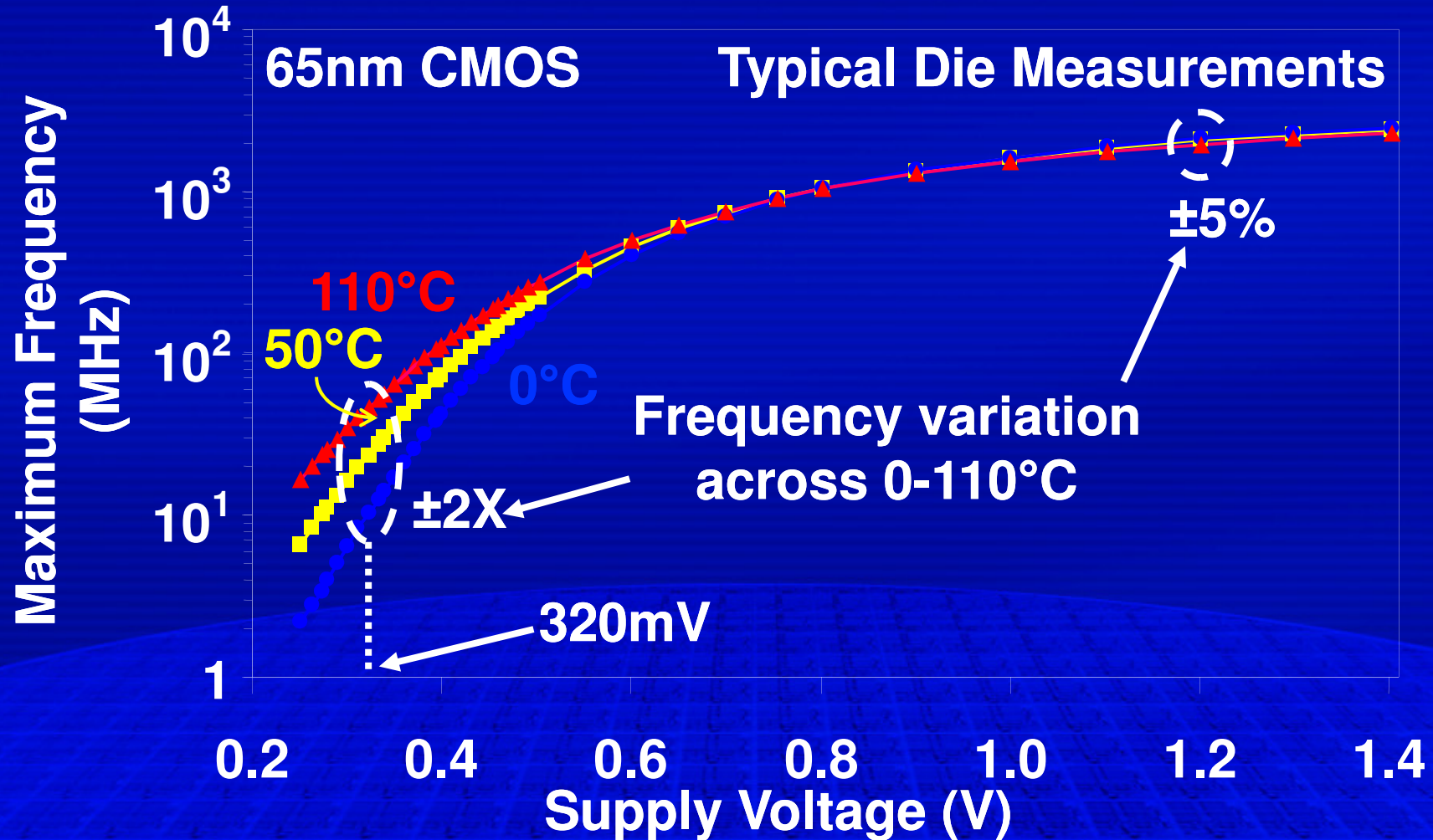


# Side Effects

- **Reduced voltage operation increases sensitivity to temperature and within die variation**
  - **RDF sensitivity of state elements is increased requiring redesign or larger sizes**
    - **SRAM  $V_{min}$  tends to increase on more aggressive technologies**
  - **Combinatorial delay variation is increased**



# Temperature Induced Variations

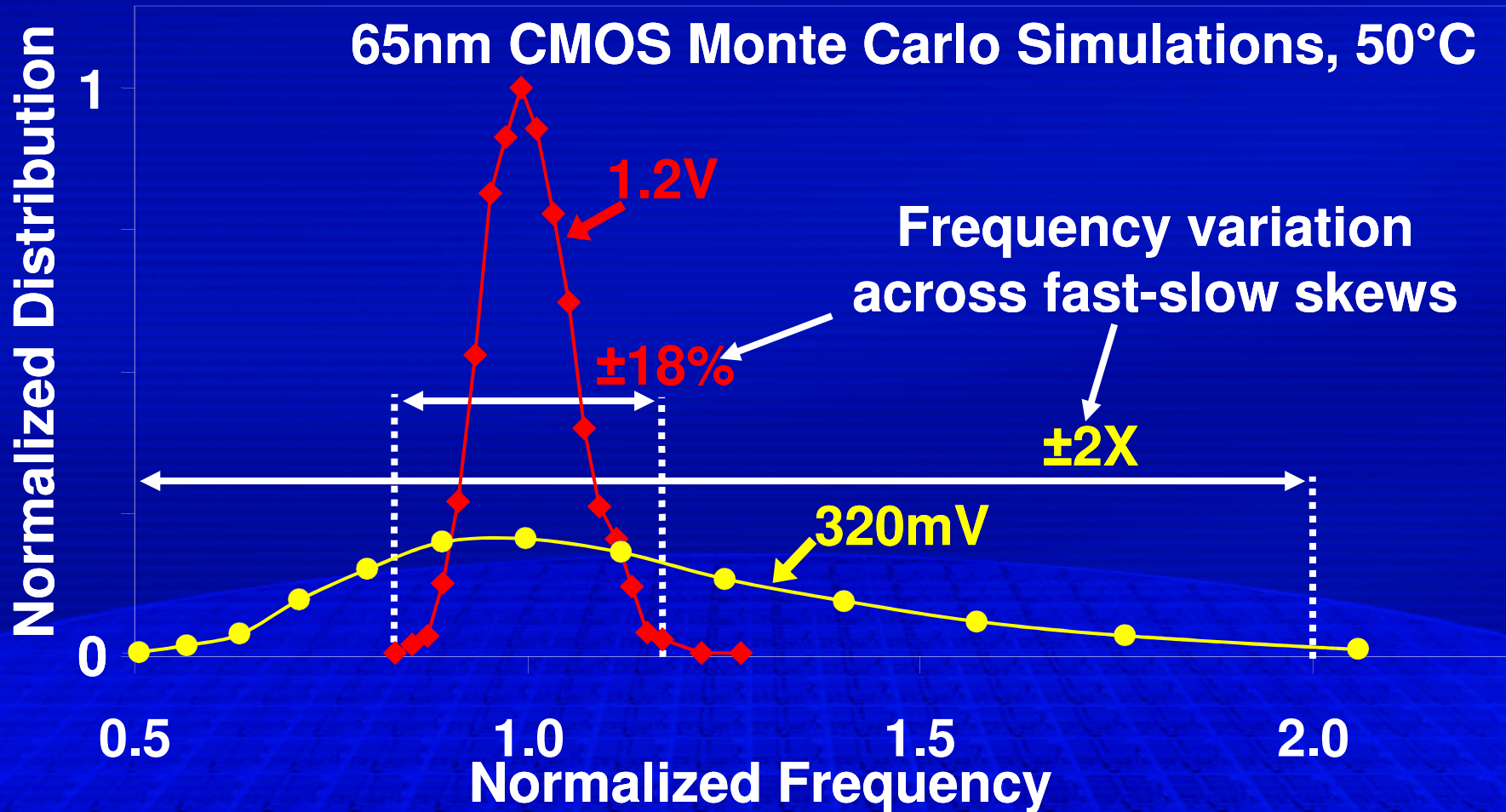


- Frequency variation across 0-110°C:

Increases from  $\pm 5\%$  at 1.2V to  $\pm 2X$  at 320mV



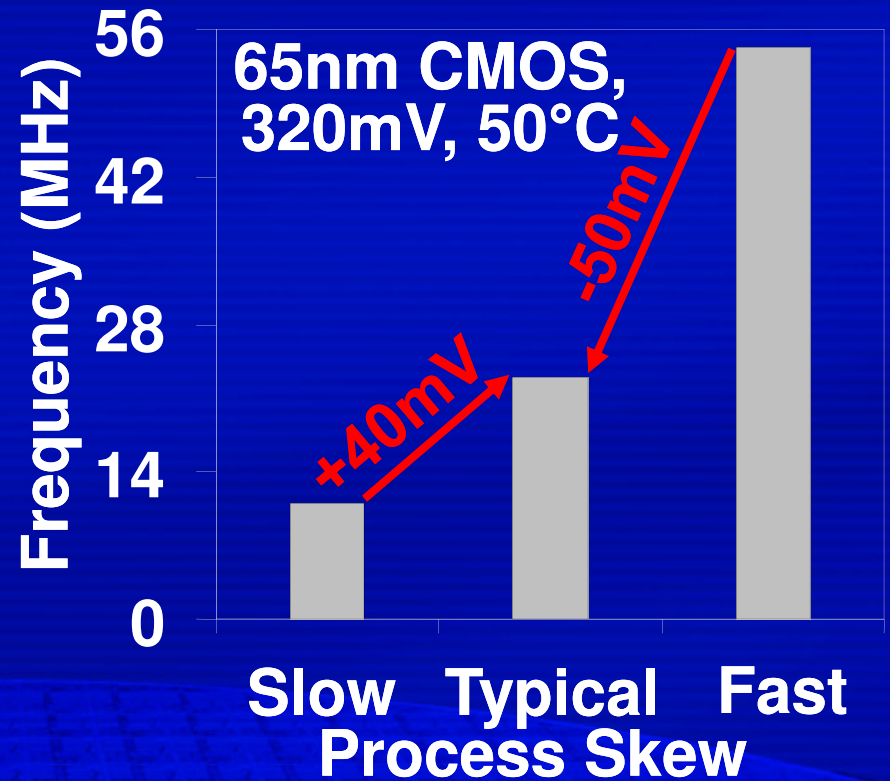
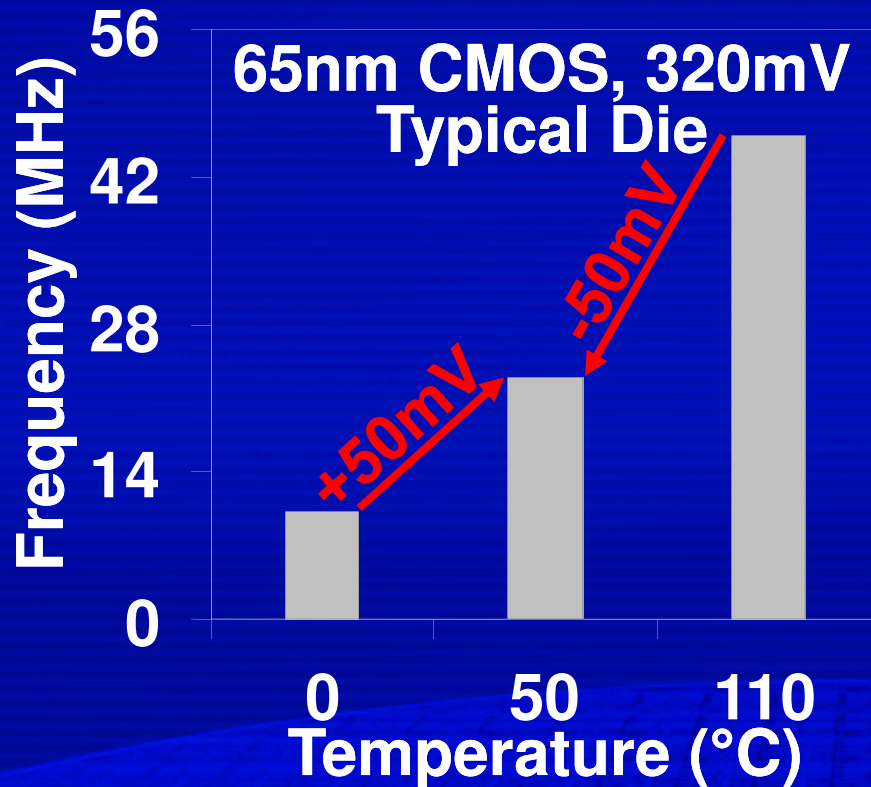
# Low Voltage Process Variations



- Frequency variation across fast-slow skews:
  - Increases from  $\pm 18\%$  at 1.2V to  $\pm 2X$  at 320mV



# Supply Voltage Compensation



- Adjust supply voltage to maintain constant performance
- $\pm 50\text{mV}$  adjustment about 320mV:  
Nominal 23MHz performance sustained across 0-110°C and fast-slow skews



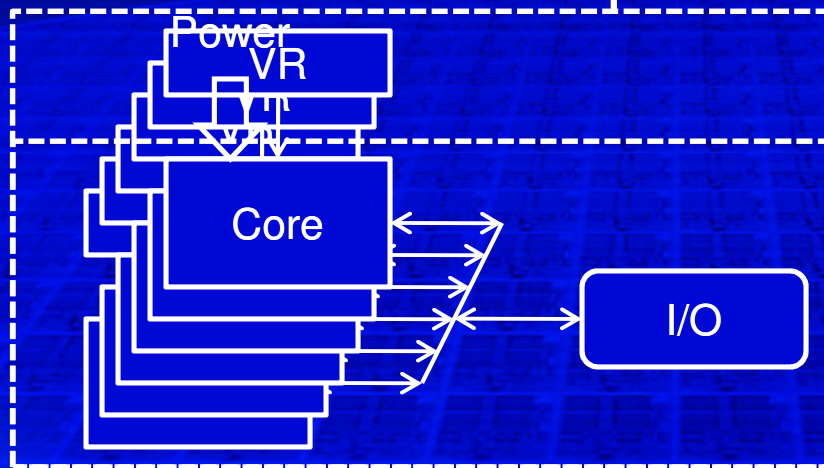
# Other Side Effects

- **Very low power delivery impedance**
- **Granularity: Each core may differ**
- **Stability of state elements:  $V_{min}$** 
  - **Some invention needed**
- **Test**
  - **Adaptation to performance,  $V_{min}$**
  - **Slowest low voltage operation is at cold**
  - **Do we need to operate across the supply range?**



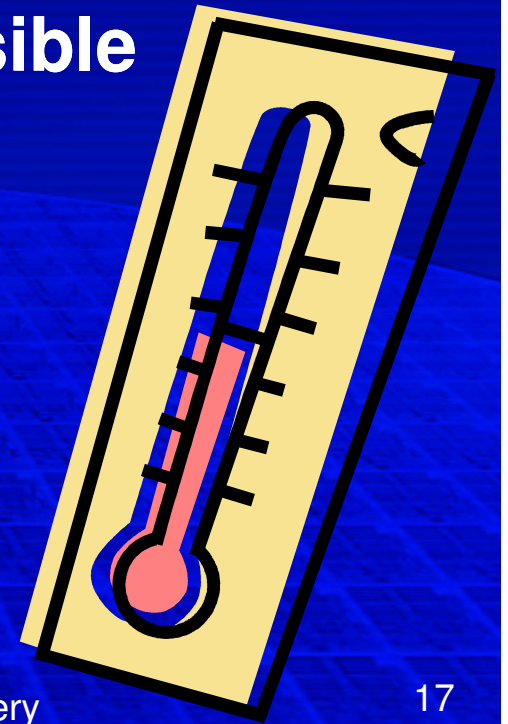
# Suggestions

- Take advantage of many cores
- Use fine grained power management to overcome within die variations
  - On die/pkg, point of load regulation
  - Adaptation is a test challenge



# How Will This Change Power Delivery?

- Regulator inefficiency moves on die
  - + Under the big heat sink
  - But the hot spot gets hotter
  - + Reducing voltage wherever possible reduces overall power



# How Will This Change Power Delivery?

- **Eliminate multiple regulators from the motherboard**
  - + Fewer components
  - + Higher voltage, lower current requirements



# How Will This Change Power Delivery?

- **Regulators are constant power loads**
  - Which means negative input impedance
  - + Power supply and package designers still have interesting work to do



# How Will This Change Power Delivery?

- **Regulators will be needed inside the die/package**
  - **Need to deal with “high” voltages and precision analog electronics on microprocessors**
  - + **New power management opportunities will arise**



# Conclusion

- **Power delivery, cooling, and variation are still challenges for many core chips**
- **Power efficient performance has become a key processor metric**
- **Operation at very low supply voltage offers significant improvement in power efficiency**
- **These combine well with the previously identified many core direction**



# Conclusion (cont)

- **Low voltage operation significantly exacerbates within die variation**
- **Distributed, on die supply regulation can compensate for this variation**
  - **Bringing new design, manufacturing, and test challenges**



# Thank You



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