

ECE260B/CSE241A - Project 3

Power Analysis of Function Blocks

Due Date: 03/07

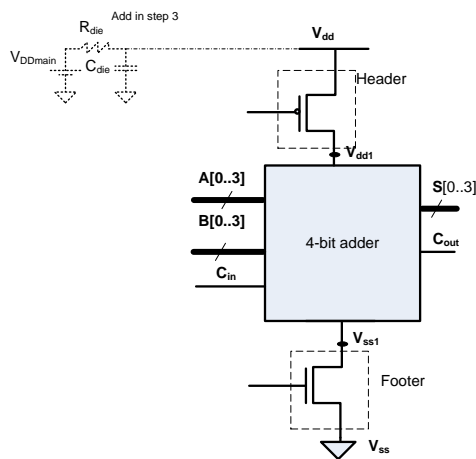
Objective: Understand the basic principle of power gating and its impact on logic. Familiarize yourself with runtime timing errors correction during low power operations.

Note: All of the following assignments are based on the PTM (predictive technology model) provided by Arizona State University, available at: <http://ptm.asu.edu/>. Needed SPICE model files and basic sample netlists will be provided. All the simulations are performed in HSpice®.

Lab Assignments:

Part 1: Impact of Power Gating on Low Power Operations

Footer and header switches are used to reduce the leakage power during standby mode. For the given 4-bit adder you can use either header switch or footer switch based on the design objective. The design should use **45nm** process. Note that the effective V_{dd} and V_{ss} of the logic is V_{dd1} and V_{ss1} . Use SPICE transient simulation w/ provided input test patterns to verify your design.



Step 1) The Objective in this step to maximize the I_{on}/I_{off} ratio for the path from V_{dd1} and V_{ss1} . We use 45nm process for this step. Based on the I_{on}/I_{off} choose the proper switch either header or footer and the proper transistor size to maximize the I_{on}/I_{off} . I_{on} and I_{off} are current through switches. Plot six different curves to justify your choice: I_{on} , I_{off} , I_{on}/I_{off} for both header and footer switch vs. transistor size with minimum 5 sampling points in the range of size [1 to 200] for plotting purpose. I_{on} and I_{off} are defined when the switch is on or off. You can use any of the vector patterns from the given input for your design and plot.

Fix your design and size for remaining steps.

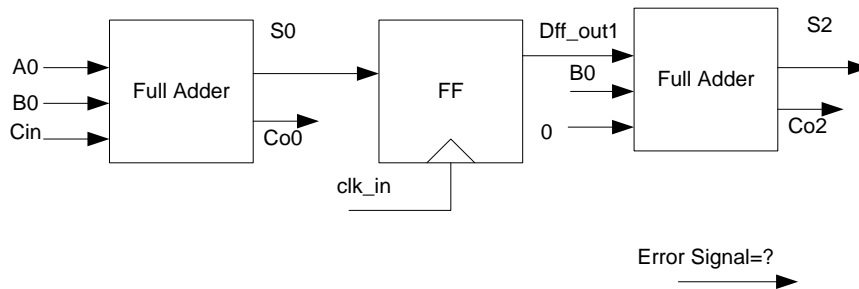
Step 2) The objective in this step is to find the product of leakage power (in switch off mode) and delay (in switch on mode) (leakage \times delay) for your switch choice in step 1. Assume delay is defined as 50% rise (fall) of the a3 (or b3) to 50% rise (fall) s3. For the delay use provided pattern for A[3..0] and B[3..0]. Compare the leakage \times delay of your step 1 switch design with ideal case with no switch (static power of the ideal case \times delay) and explain the trade offs in each one.

Step 3) In power gating the effective voltage over logic ($V_{\text{eff}}=V_{\text{dd}}-V_{\text{ss}}$) is changed from ideal V_{dd} and V_{ss} to V_{dd1} and V_{ss1} as shown in the figure. In this section, we add the parasitics of a non-ideal power distribution lumped model to your step 1 design V_{ddmain} as provided in the netlist and figure. Add both R_{die} and C_{die} to V_{ddmain} . Measure the V_{eff} for the footer or header switches that you designed in step 1. How does the leakage power, delay, leakage \times delay and V_{eff} changed as compared to step 1 choice with and without none ideal voltage supply.

Step 4) Study the impact of technology scaling on the power/performance of the power gating. Simulate the same design in step 1 using 65nm and 32nm process, and collect all the data you measured in Step 2). Put all the leakage \times delay in a table and discuss the performance trend of such power gating w/ technology scaling.

Part 2: Timing Error Detection with RAZOR

RAZOR architecture is adopted to tally and integrate the errors per clock cycle occurring in the data path. The goal of this section is to design RAZOR architecture to detect the timing error. The FF samples wrong value. Extra credit is for error correction step. We use 45nm process for this part. Out put of the first full adder s0 is passed through the main FF to the next stage adder and used as an input to Full adder 2:



Step 1) Design the proper RAZOR architecture based on the provided timing to detect the timing error on the first stage Logic stage1. Add the needed circuit and clock timing to detect error. The correct output dff_out1 that needs to be sampled by the main FF is '1', however due to clock variation, the FF output dff_out1 samples '0' values. Describe your design and provide the needed waveforms and demonstrate the raise of the error flag due to the error. You can use either FF or latch in your error detection.

Step 2) Show the waveforms and error flag in your RAZOR design in step 1 under voltage scaling when the voltage scales from 1.2V down to 0.8 with steps of 0.2V. If needed adjust clock delay in detection.

Step 3) Show the functionality of your RAZOR error detection architecture in step 1 under temperature variation for three different values -30C, 25C and 125C.

Step 4) Measure and report the total power (dynamic and leakage) overhead due to your RAZOR design in step 1.

Step 5) Adopt your same design in step 1 and change the process to 32nm and 65nm and describe the impact of process scaling on your error detection.

Extra Credit: Based on your error detection circuitry and timing, use mux 2:1 of your choice and your error flag to inject the correct value into the FF. Demonstrate the proper signal waveforms to show error correction.

Report Requirement:

1) Clearly show your results step by step with necessary figure illustrations.

2) Discuss and comment your results concisely.

Notice:

Needed SPICE models and sample netlists are in public directory: ../public/LAB3. Be sure to use the SPICE models we provided in the directory LAB3/ptm_lib. DO NOT use the SPICE models in ptm_lib of LAB1.