

# ECE260B/CSE241A

## Project 1

- Power Analysis of Combinational Logic Gates

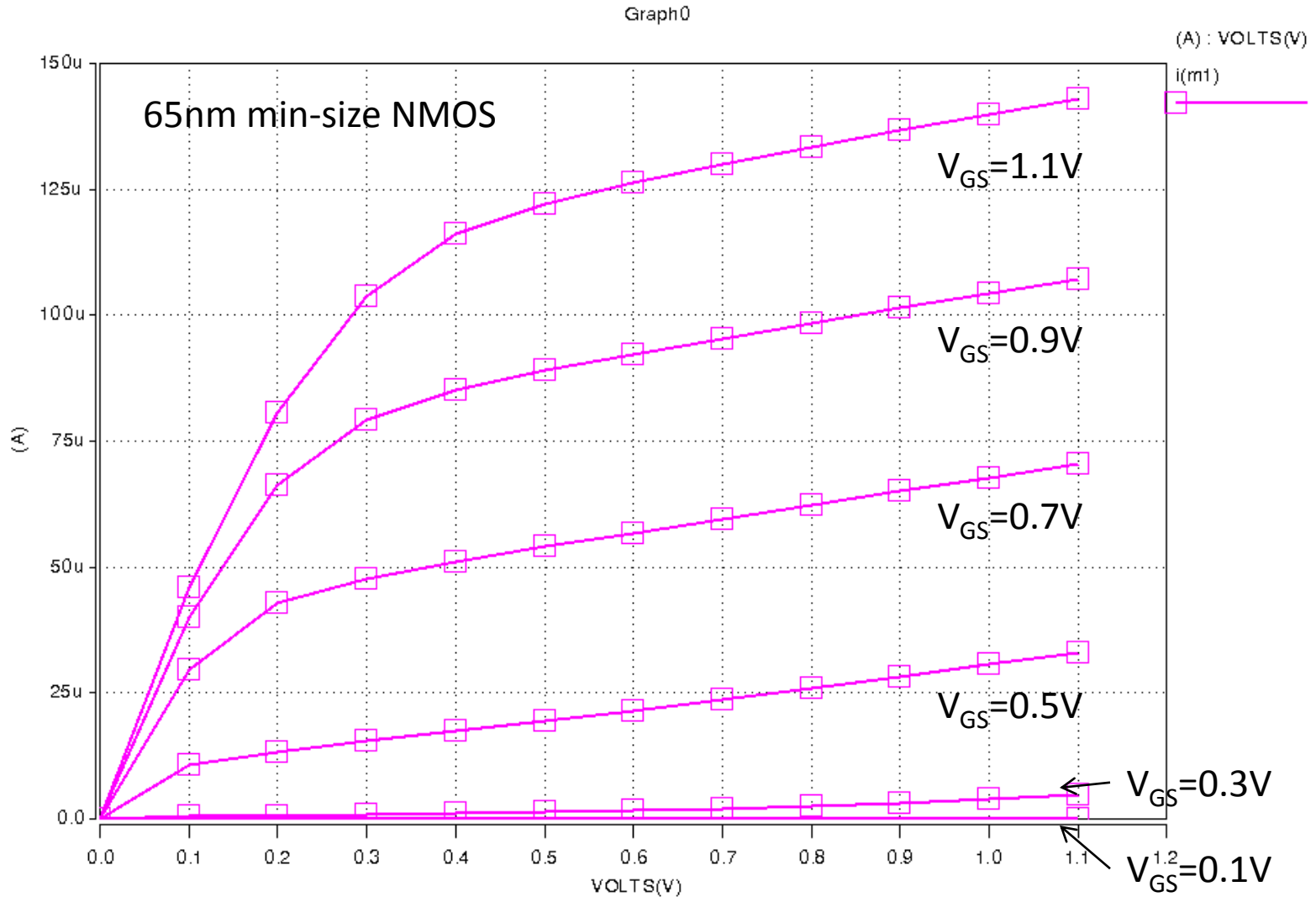
Yulei Zhang

2010/01/19

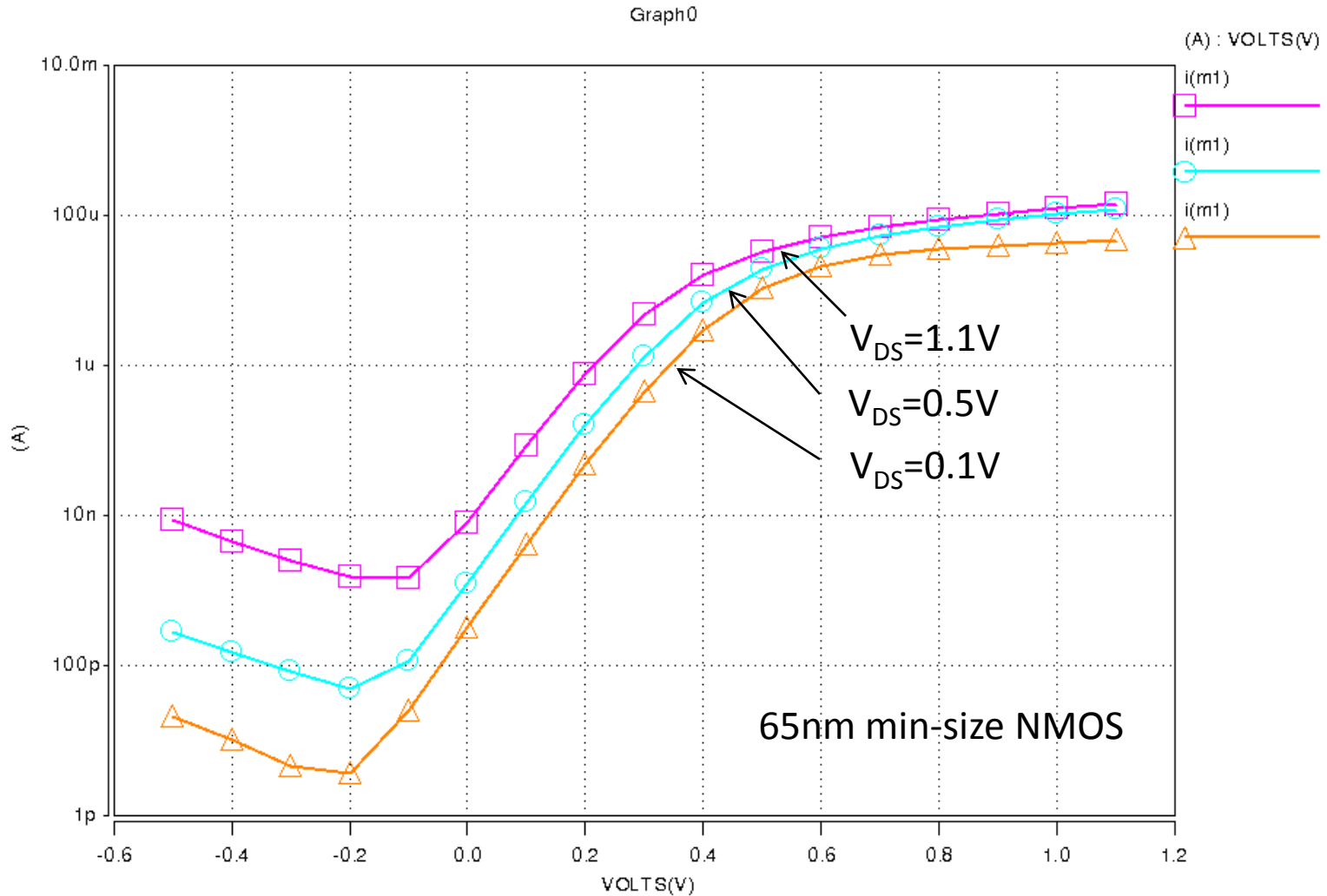
# Agenda of Project 1

- Part 1: Study  $I_{ON}$  and  $I_{OFF}$  (leakage) of single transistor.
  - I-V characteristic of transistors.
  - Study of leakage current.
  - Impact of technology scaling (65nm~32nm) on  $I_{ON}/I_{OFF}$ .
  - Side effects: temperature, body biasing.
- Part 2: Study E-D trade-off of a loaded inverter.
  - Plot E-D trade-off curves for different inverter sizes/different voltages.
  - Discuss how to choose the best size/ $V_{DD}$  for given delay constraint.
- Part 3: Detailed power analysis of combinational logic gates.
  - Design gate size to achieve similar performance. (logical efforts)
  - Show how to choose the better logic option in terms of energy.
  - Measure static/dynamic power dissipation for different technologies.

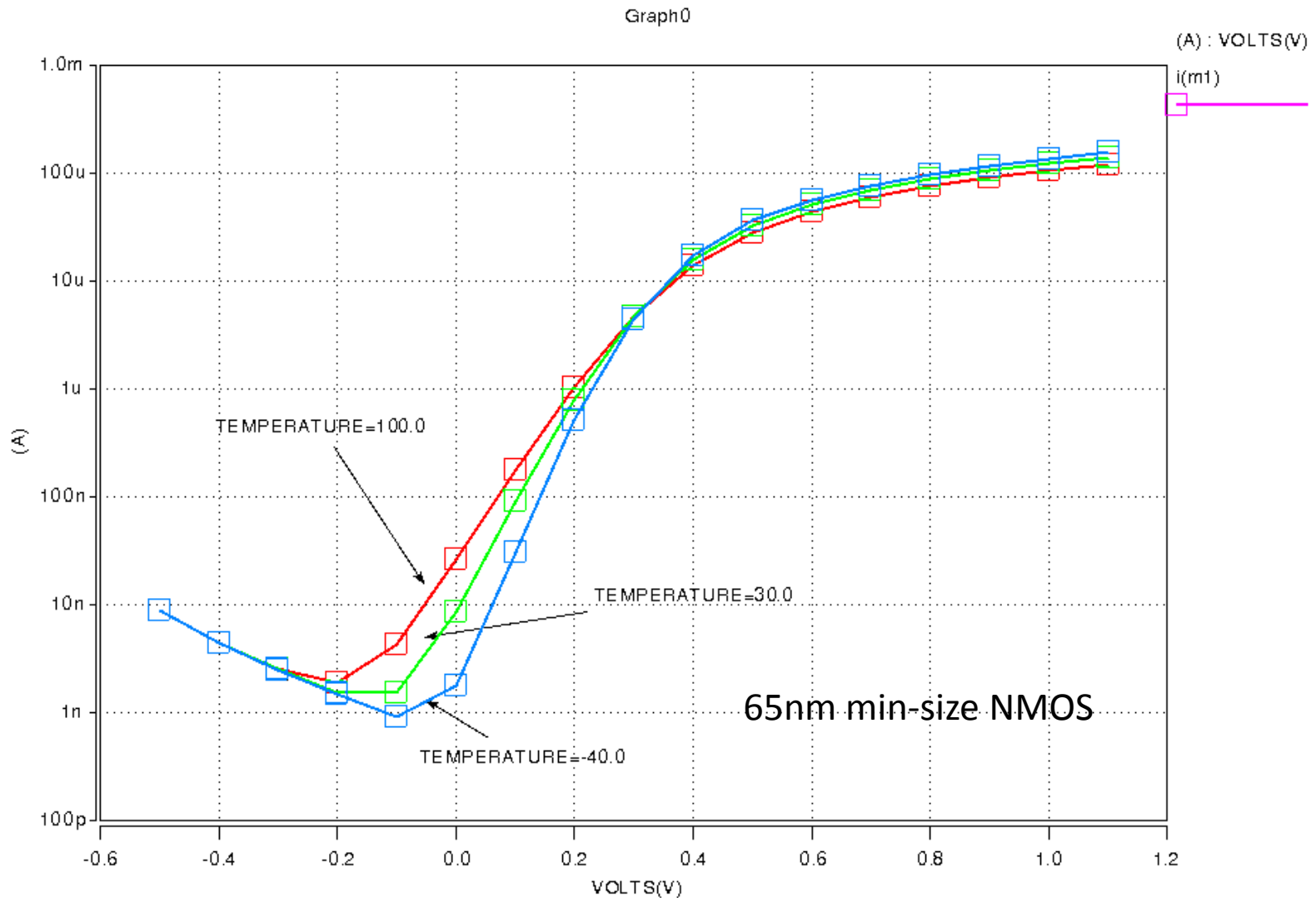
# Part1 – I-V characteristic of MOS transistors



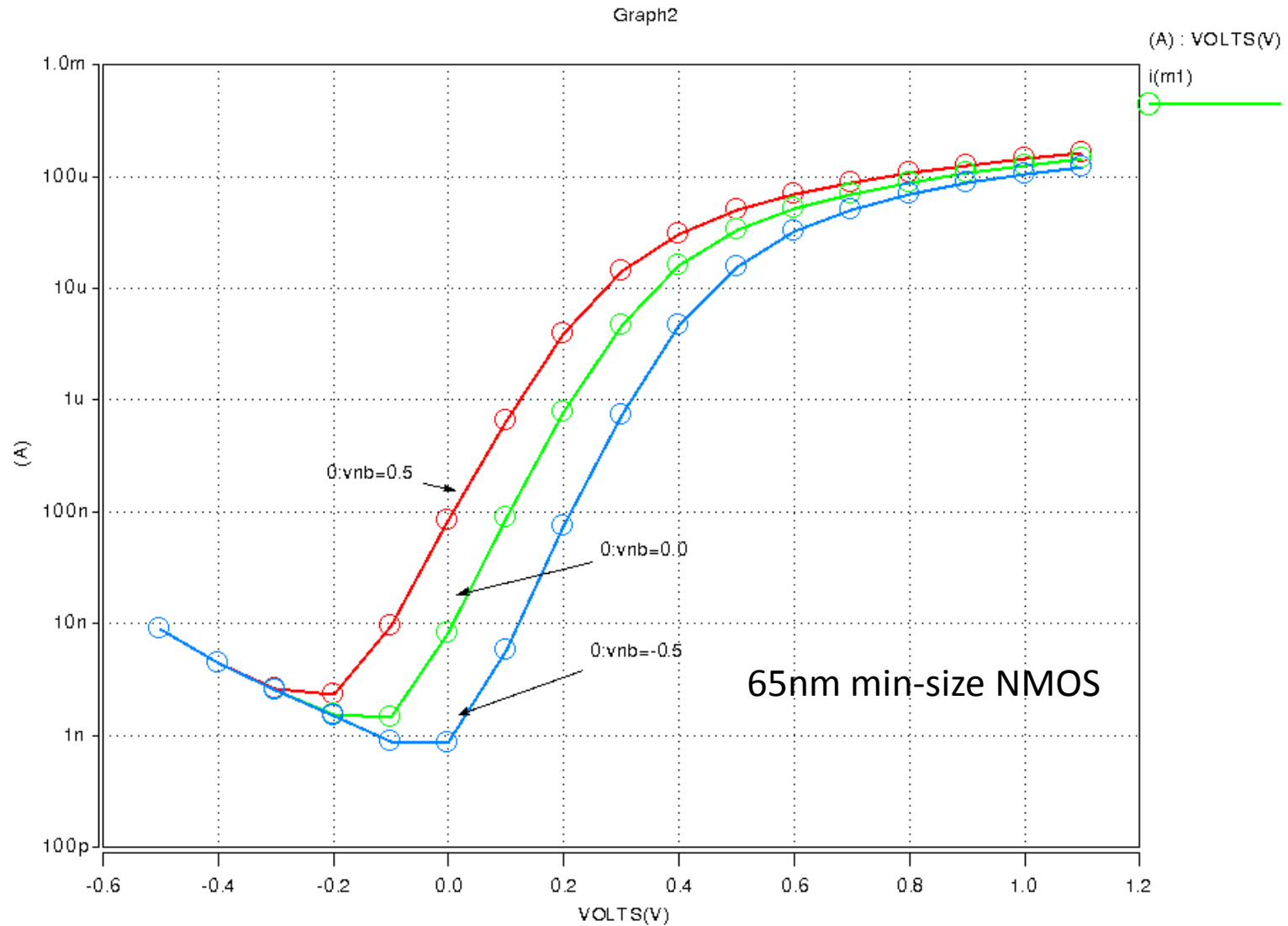
# Part 1 – Study of all leakage effects



# Part1 – Study of temperature effects



# Part1 – Study of body biasing





# Part3 – Power analysis of combinational logic gates

