

# ECE260B/CSE241A - Project 1

## Power Analysis of Combinational Logic Gates

**Lab Posted: 1/8 (Friday) Due Date: 1/26 (Tuesday)**

**Objective:** obtain an overview on how the power (dynamic and leakage) is consumed in transistors and simple logic gates, also get familiar with the energy-delay trade-off in the low-power design.

**Note:** All the following assignments are based on the PTM (predictive technology model) provided by Arizona State University, available at: <http://ptm.asu.edu/>. Needed SPICE model files and some sample netlists will be provided. All the simulations are performed in HSpice®.

### **Lab Assignments:**

#### **Part 1: Study the $I_{on}$ and $I_{off}$ of a single transistor**

For a min-sized single CMOS transistor w/ 4 terminals (Gate, Drain, Source, and Body) controlled by voltage sources, perform the following steps:

**Step 1)** Show the I-V characteristic of a 65nm PMOS and NMOS transistor where  $V_{DS}$  ranges from 0 to 1.1V incrementing by 0.1V for five  $V_{GS}$  values increment by 0.2V between 0.1V and 1.1V. Draw the I-V curve.

**Step 2)** Show all the leakage effects of a 65nm CMOS transistor (PMOS and NMOS) where  $V_{GS}$  varies from -0.5 to 1.1V incrementing by 0.1V for three  $V_{DS}$  values between 0.1 and 1.1V incrementing by 0.5V. Draw the I-V curve.

**Step 3)** Show the temperature effect on the current of a 65nm CMOS transistor (PMOS and NMOS) by drawing the same I-V curve as in Step 2) with  $V_{DS}$  fixed at 1.1V but for three temperature settings: -40C, 30C, 100C.

**Step 4)** Show the biasing effect on the current of a 65nm CMOS transistor (PMOS and NMOS) by drawing the same I-V curve as in Step 2) with  $V_{DS}$  fixed to 1.1V but using three body biasing voltages: -0.5V, 0, 0.5V.

**Step 5)** Give a table to summarize the  $I_{on}$ ,  $I_{off}$ , and  $I_{on}/I_{off}$  of min-sized PMOS/NMOS transistors for 65nm, 45nm, 32nm process technology nodes. For this step, assume no body biasing and temperature is fixed at 30°C.  $V_{GS}$  is  $V_{DD}$  when simulating  $I_{on}$  and 0 when simulating  $I_{off}$ , while  $V_{DS}$  is always equal to  $V_{DD}$ .  $V_{DD}$  is assumed to be 1.1V, 1.0V, and 0.9V for 65nm, 45nm, 32nm process, respectively according to the ITRS roadmap.

#### **Part 2: Study Energy-Delay trade-off of a loaded inverter**

For a single inverter in 45nm process driving a 100fF on-chip capacitance, performing the following steps:

**Step 1)** Plot the Energy-Delay (E-D) trade-off curves of such circuitry for three inverter sizes: 10×, 50×, 100× of min-sized inverter and three supply voltages 0.6V, 1.1V, 1.5V. Finally, you should have at least 6 different E-D curves plotted on the single figure. Make sure to label the different curves. The X-axis and Y-axis of this figure should be delay and energy, respectively.

**Step 2)** Discuss how to choose the Optimum inverter size/supply voltage based on some specific performance requirement (e.g. delay should be less than 20ps, 40ps, 60ps, etc).

### ***Part 3: Detailed power analysis of combinational logic gates***

In order to design an AND4 logic gate in 45nm to achieve the low-power (driving the same 100fF cap), we end up with two options: A) NAND4+INV; B) 2 NAND2 + NOR2. Perform the following steps to compare these two options:

**Step 1)** Design the gate sizes to achieve similar performance (delay) for these two options. (Hint: based on the calculation of logic efforts.)

**Step 2)** Based on Energy-Delay performance which option you choose (A or B)? Please justify your choice.

**Step 3)** Characterize the dynamic/static power dissipation of these two options using three different processes: 65nm, 45nm, 32nm and give a table to present your results. For static power evaluation, it should be calculated by averaging the leakage power at different patterns (totally 16 patterns for AND4), and for dynamic power evaluation, just subtract the leakage value from the total power simulated (using the input dynamic pattern we provided in the netlist).

#### **Report Requirement:**

- 1) Clearly show your results step by step with necessary figure illustrations.
- 2) Discuss and comment your results concisely.

#### **Lab Environment Setup:**

Lab is located in **EBU1-5702**, or you can remotely SSH to the following server: [ieng6.ucsd.edu](http://ieng6.ucsd.edu) by using your username and password.

**Notice:** You need to remotely ssh using: `ssh -X username@server` to enable launching display and GUI.

After log in and before running the experiments:

1. Change to c-shell (csh) → type: `tcsh`
2. Source setup : `source ../public/setup`

in the linux prompt, to get your simulation environment ready. To invoke the HSPICE, just type

`hspice *.sp`

to run the SPICE simulations.

You can use `cscope` to view your simulation waveforms by typing:

`cscope &`

in the linux shell.

**Notice:** Needed SPICE models and sample netlists are located in public directory → `../public/LAB1`