ECE260B/CSE241A – Final Project

Designing Low Power 16-bit Adder

Due Date: Midnight 03/19

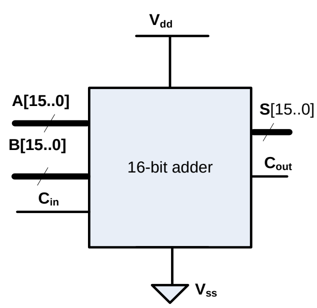
Objective: Understand the principles of designing low power function blocks. Applying low power techniques to design a function block.

Note: All of the following assignments are based on the PTM (predictive technology model) **32nm** technology provided by Arizona State University, available at: http://ptm.asu.edu/. Needed SPICE model files, interface and input vectors will be provided. All the simulations are performed in HSpice®.

Project:

Designing Low Power 16-bit Adder Module

The goal of the project is to design a low power 16-bit adder. You can apply any low power design techniques of your choice to design the 16-bit adder. The goal of the project is to minimize "**Total energy × Total delay × Total area**" in your adder design which is your design metric. You will compete with other groups to minimize your design metric. Group with the minimum metric will get the full credit and the rest of the groups are ranked accordingly. The design should use **32nm** process. Use provided input test vector patterns to verify your design.



Adder Design) Design your 16-bit adder. You can design your adder with any low power design technique of your choice. You can design an either synchronous or asynchronous adder. The objective of your design is to minimize "***Total energy* × *Total delay* × *Total area***" for the two sets of input patterns totally.

Input Vector Patterns) You design single adder cuircuitry that switches between the input sets and choose the proper vectors for both test case I and II. You should use same circuit adder for both test cases. You will simulate your 16-bit design adder with provided two input sets:

> ***(Test case I) Sum of Twenty pairs of inputs*****:** 20 pairs of 16-bit input vectors are added.
>
> ***(Test case II) Sum of Twenty inputs all together*****:** 20 16-bit input vectors are added all together**.**

Please copy updated test patterns from ../public/Final_Project

Design Metric) Your goal is to minimize *Total energy* × *Total delay* × *Total area* in your 16-bit adder design. This design metric is used to evaluate the performance of your adder design.

1. **Total Energy (unit: pJ):** The total energy is the total average dynamic and static energy (average power × cycle time) consumed to finish computation of all the test case I and II to the end.
2. **Total Delay (unit: ns):** The total delay is the total time to finish computation of all the test case I and II to the end and have the last bit of the last summation ready. Delay is computed based on the 50% rise (fall) of the first input to the 50% rise (fall) of your last output at the end of the test case I and II.
3. **Total Area (unit: um):** The total area is the total area of your adder. In your design, the length of the transistors L is fixed (32nm). You can use any width W of your choice in your adder design. You will calculate the area estimation by adding all the transistor width together.

Grading Policy:

The final project report has total of 20 points. You will compete with other groups designed adder to minimize the *Total energy* × *Total delay* × *Total area* design metric for the total computation of test case I and II. **In your final project, report your adder design metric *Total energy* × *Total delay* × *Total area* (pJ*ns*um) in the beginning of your report before you begin your main report.**

The report grading policy is:

(5 points): Describe your adder design circuit and methodology and technique you adopt to reduce the design metric *Total energy* × *Total delay* × *Total Area.*

(10 points): Your adder design should provide correct result for both test cases I and II (pass the test using provided patterns). Provide the waveforms and/or vectors that demonstrates your adder is functional for test case I pairs and test case II total numbers. Attach netlist of your design in the appendix.

(5 points) Competition points: You will compete with rest of the groups to minimize design metric *Total energy* × *Total delay* × *Total area*. The group with the minimum *Total energy* × *Total delay* × *Total area* will get 5 points score in this section and the group with maximum design metric will get 0 point score. The rest of the groups will be normalized between 0 to 5 points. Your goal is to minimize the design metric as much as possible.

(Bonus points): First top three groups with the minimum design metric *Total energy* × *Total delay* × *Total area* will receive additional **3, 2 and 1 points** respectively added to the total 20 points of project.

Report Requirement:

1) Report your design metric in the beginning of your report.

2) You need to have single adder circuitry design and select the correct vectors using your adder design.

3) Report total power of all Vdds and area of all of your circuits. Do not exclude any part of your circuits.

4) Send your netlist file with your report to TAs. We will use it to test your design.

5) Report three timing points: (i) Time to finish test case I (ii) and test case II and (iii) all the test cases.

6) Discuss and comment your results concisely with needed figures and illustrations.

Notice:

Needed SPICE models and sample netlists are in public directory: ../public/Final_Project. Be sure to use the SPICE models we provided in the directory Final_Project/ptm_lib. DO NOT use the SPICE models in ptm_lib of LAB1.