

ECE260B/CSE241A Exercise February 12, 2010

Exercise 1. Scaling Trend:

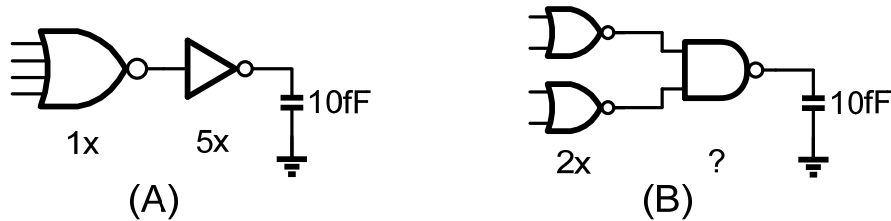
Describe the scaling trend of delay, power, and energy per instruction according to the following model. Depict your assumptions.

- 1) Conventional long channel model.
- 2) Short channel model.
- 3) ITRS roadmap.

Exercise 2. Logic Effort Calculation.

In order to implement OR4 logic in 45nm process to drive a 10fF on-chip capacitance, we end up with two options, (A) NOR4+INV; (B) 2 NOR2 + NAND2, as shown below. Assuming sizes of all the logic gates are tuned to follow the inverter with 2:1 P/N ratio and per unit width gate capacitance $C_{\text{perwidth}}=1.5\text{fF}/\mu\text{m}$.

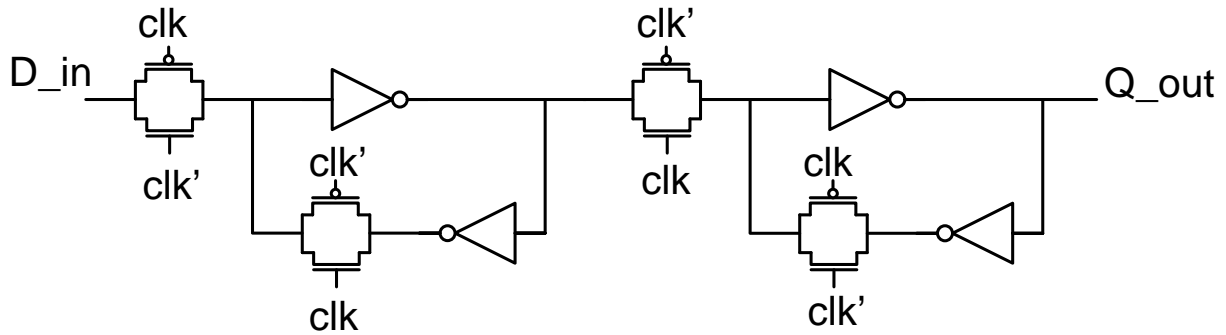
- 1) Calculate the size ratio of NAND2 in option (B) to make (A) and (B) achieve the same delay. (neglect all the parasitic capacitance during calculation and the minimum CMOS transistor width $W_{\text{min}}=2L$, where L is the feature size.)
- 2) Which option saves more dynamic power, and why?



Exercise 3. Flip-Flop Analysis.

For the conventional master-slave D flip-flop design shown below,

- 1) Explain the basic working principle of this flip-flop.
- 2) Analyze the setup time T_{setup} and clock-to-q time $T_{\text{C-Q}}$. Give simply formulae to describe the values of T_{setup} and $T_{\text{C-Q}}$ using delay of the inverter and delay of the transmission-gate. (Assume all the inverters have the same delay and so do transmission-gates.)



Exercise 4. Energy-Delay Tradeoffs.

If the drain current of a saturated CMOS transistor can be described using α -power current law, the delay of a logic gate can be modeled as:

$$Delay = K \frac{CV_{DD}}{(V_{DD} - V_{TH})^\alpha}$$

where K is a fitting coefficient and C represents the loading capacitance of such logic gate. Assuming dynamic power is dominant in such logic gate, the energy dissipation is CV_{DD}^2 .

- 1) Calculate the optimal V_{DD} to achieve the lowest energy-delay product.
- 2) Calculate the optimal V_{DD} to achieve the lowest energy-delay² product.
- 3) Discuss the trend of V_{DD} by comparing the results of 1) and 2).

Exercise 5. Activity Factor Calculations.

The And-Or-Invert (AOI) gates are often included in the standard cell library to reduce the area of synthesized combinational logic. For the AOI function $Y = \overline{A \cdot (B + C + D)}$

- 1) Write down the truth-table for the output Y , and calculate the activity factor $\alpha_{0 \rightarrow 1}$ for the output assuming all the inputs are independent and uniformly distributed.
- 2) Draw the simplest possible implementation of this logic function using 2-input basic gates (NOR, OR, NAND, AND, XOR) and compute the activity factors for all the internal nodes and output node.
- 3) Discuss which implementation saves more energy, and why?

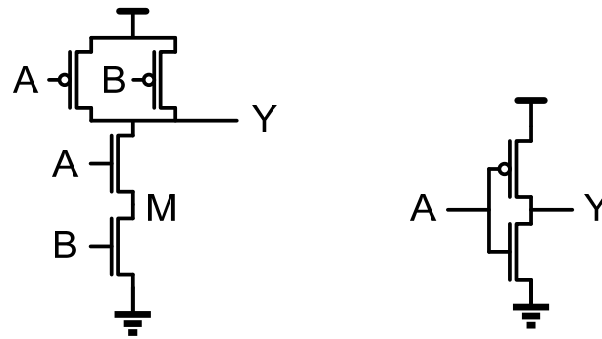
Exercise 6. Leakage Current

Suppose the leakage current of a single transistor can be expressed as,

$$I_{leak} = I_0 10^{\frac{V_{GS} - V_{TH} + \lambda_d V_{DS}}{S}}$$

where $\lambda_d = 0.1$ is the DIBL factor, and $S = 100mV$ is the sub-threshold swing. For the NAND2 and INV implementations shown blow (assume $V_{DD}=1V$),

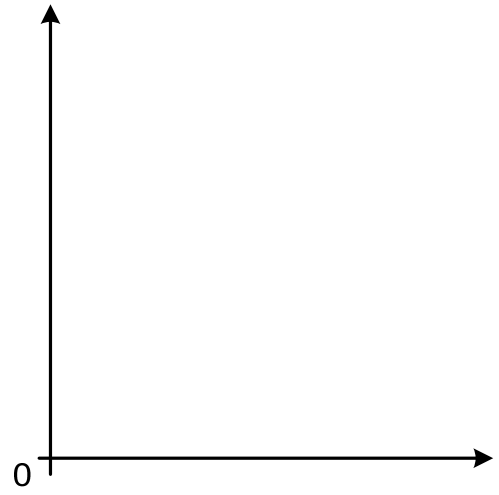
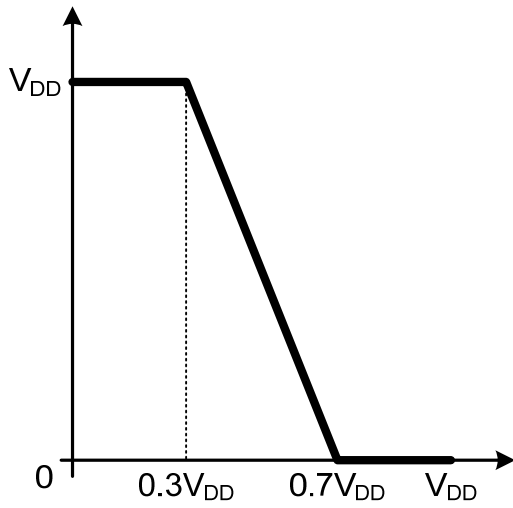
- 1) Calculate the voltage value V_M at the node M, when $V_A=V_B=0$ in the NAND2 gate.
- 2) Calculate the leakage reduction ratio $I_{leak,NAND} / I_{leak,INV}$ of NAND2 gate compared with the INV gate, when $V_A=0$ in the INV gate.



Exercise 7. 6T-SRAM Analysis.

To study the reliability of a 6-T SRAM cell design, we break up the back-to-back inverter loop and simulate the voltage transfer characteristic of one inverter in the hold-mode by setting $WL=0$. The VTC curve is given blow.

- 1) Draw the butterfly plot of hold-mode (on the right blank figure) and calculate the SNM (Static Noise-Margin), assuming $V_{DD}=1V$.
- 2) If due to the process variation, the VTC curve is shifted to the left (vice versa for another inverter) by 50mV when V_{DD} drops by 100mV, calculate the DRV (data retention voltage) value.



Exercise 8. Aggressive Scaling

Describe the strategy of Razor Project. What will be the key issues when we implement the strategy for the following designs?

- 1) General purpose processors,
- 2) ASICs,
- 3) FPGA.