Midterm 1 Preview

This is a non-exhaustive example of what might be on your midterm.
• Given a cache configuration (e.g.: 32KB, 2-way, 16b lines, LRU replacement)
  • Estimate (as precisely as possible) the data hit rate for a given code sequence
  • Estimate (as precisely as possible) the impact of increasing associativity
  • Estimate (as precisely as possible) the instruction hit rate for a given code sequence.
  • How would adding a trace cache affect the miss rate? The number of misses/instruction executed?
  • What fractions of the misses will be conflict, capacity, compulsory.
• Describe the purpose and operation of a victim buffer.
• Would the impact be of adding a victim buffer to the TLB and why?
• Describe 2 two reasons for the shift from RISC to CISC
• What is VLIW? What makes VLIW machines hard to compile for?
• Would you expect a VLIW machine to exhibit better or worse i-cache behavior than a RISC machine? Why?
• You should be able to look at simple C code and reason about stream of loads and stores will generate.
• Know how DRAMs and SRAMs work and the tradeoffs involved.