Computer Architecture Review

or

*CSE 141’s Greatest Hits*

-- ISA types
-- ISA formats and tradeoffs
-- addressing modes
-- branch types
-- MIPS ISA

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Instruction Set Architecture

• What we learned
  – speedup
  – execution time
  – ET = IC * CPI * CT
  – Amdahl’s law

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Performance

• What we can do
  – identify and write simple code for various ISA types
  – identify and use several addressing modes (MIPS types, particularly)
  – write MIPS code (with cheat sheet)
  – encode or decode MIPS code to/from machine language
  – evaluate tradeoffs between ISAs

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Performance

• What we can do
  – calculate CPI, ET, clock-rate, etc.
  – calculate speedup
  – apply Amdahl’s law

Computer Arithmetic

• What we learned
  – the computer uses binary numbers
  – number systems
  – negative numbers
  – addition, subtraction, multiplication, division
  – ALU design
  – floating point numbers, operations

Computer Arithmetic

• What we can do
  – manipulate binary numbers
  – do arithmetic on binary numbers
  – do arithmetic on fp numbers
  – ALU design

CPU Architecture

• What we learned
  – single-cycle cpu, multiple cycle cpu
  – datapaths
  – control logic
  – multiple-cycle control
    • FSM
  – exceptions
CPU Architecture

- What we can do
  - construct datapath for new instructions
  - generate control logic for new datapath or new instruction.
  - incorporate exceptions into datapath and control

Pipelining

- What we learned
  - pipelined machine design, including
    - use of intermediate registers
    - pipelined control
  - data hazards, bubbles, and forwarding
  - branch hazards, bubbles/flushing, and simple branch prediction
  - advanced architectural concepts including branch prediction, superscalar execution, superpipelining, and out-of-order execution.

Pipelining

- What we can do
  - design a slightly different pipelined machine
  - generate control for it
  - understand implications of all kinds of data hazards
  - understand implications of all kinds of branch hazards
  - reason about instruction schedules for pipelined, superscalar, out-of-order, or VLIW machines

This pipeline is designed to eliminate the ld-use data hazard of the MIPS pipeline. Does it? Assume address calculation is done in addr, and all other alu operations are done in ex. What other hazards does it create? Show all bubbles and forwarding for the following code:

```assembly
lw  R3, 100(R6)  if   id   addr   mem   ex   wb
add R5, R3, R2  if id
sw R5, 200(R6)
sub R7, R1, R3
lw  R4, 500(R7)
```
Memory

• What we learned
  – locality
  – memory hierarchies
  – hits, misses, miss penalties
  – cache performance (miss rates, MCPI, ET)
  – write-through, write-back, write-allocate, write-around
  – Associativity
  – Cache block size
  – Compulsory, capacity, conflict misses
  – Virtual memory

• What we can do
  – identify types of locality, types of misses (compulsory, capacity, conflict)
  – identify hits and misses and manipulate cache structures for all types of caches
  – evaluate or predict cache performance
  – do LRU replacement

Multiprocessing & Multithreading

• What we learned
  – Classifications
    • SISD, SIMD, MIMD
    • Bus/network
    • UMA/NUMA
    • Shared memory/message passing
  – Cache Coherence Problem
  – Cache Coherence Protocols
  – Multithreading models
    • Fine-grain
    • Coarse-grain
    • Simultaneous Multithreading (SMT)

11. (5 points) A 256 KB cache interprets addresses this way. What is the associativity of this cache? (Addresses are byte addresses)
Multiprocessing & Multithreading

• What we can do
  – Discuss MP, MT types and their tradeoffs
  – Think about cache coherence protocols and tradeoffs