Objective
- Get familiar with the Xilinx ISE webpack tool
- Learn how to design basic combinational digital components
- Learn how to simulate

Please note:

For this lab assignment, you will work alone and use schematics as input to simulation. Before you begin, please take a look at tutorials that are in the following directory:
http://cseweb.ucsd.edu/classes/wi10/cse140L/labs/lab1/

Tutorial1.pdf: Step by step example of schematic flow design with ISE9.2i

Tutorial2.pdf: More examples in using the schematic flow design

Part of the tutorial focus is on how to use the bus object as part of the design to reduce the complexity and improve the verification process. We expect you to use the bus object in this lab when needed.

Part 1: 7-segment display decoder

For a given input that is in the range of 0 - 15, design a circuit that outputs the hexadecimal number on the 7 segment display. For example, all outputs other than G are high for an input of 0.

**HINTS:**
Number 6: High- A,C,D,E,F,G  Low- B
Number B: High- C,D,E,F,G  Low- A,B
Number D: High- B,C,D,E,G  Low- A,F

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>W X Y Z</td>
<td>A B C D E F G</td>
</tr>
<tr>
<td>0 0 0 0</td>
<td></td>
</tr>
<tr>
<td>0 0 0 1</td>
<td></td>
</tr>
<tr>
<td>... ... ...</td>
<td></td>
</tr>
<tr>
<td>1 1 1 0</td>
<td></td>
</tr>
<tr>
<td>1 1 1 1</td>
<td></td>
</tr>
</tbody>
</table>

Report:
a) Truth table of the 7 segment decoder using table format give above
b) Boolean expression you derived from the truth table.
c) Circuit schematics
d) Screen snapshot of the 7-segment decoder output when the input changes from 15 to 0.
**Part 2: Adder/ Subtractor**

Implement a circuit that performs the following function on a two 4-bit input numbers (X, N):

<table>
<thead>
<tr>
<th>Input(X)</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>X is odd number</td>
<td>X - N</td>
</tr>
<tr>
<td>X is even number</td>
<td>X + N</td>
</tr>
</tbody>
</table>

Design this circuit using minimal logic. The building components of your addition circuit should be composed of a 1-bit full adder and other logic as necessary (the 1-bit full adders are available in the tool library).

**Report**

a) Show the design steps including the truth table  
b) Circuit schematics  
c) Results: Include one screen snapshot of the simulator outcome for the following input combinations  
   X = 8 and N = 7  
   X = 15 and N = 8

**Part 3: Selective encoder**

In this part you will be implementing a circuit that performs selective encoding on a 3-bit binary input. The user can select among the available encodings with two selective switches (S0, S1) as follows:

<table>
<thead>
<tr>
<th>Input: X</th>
<th>Selective switches (S0, S1)</th>
<th>Encoding scheme: Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-bit input (X2, X1, X0)</td>
<td>00</td>
<td>Gray code</td>
</tr>
<tr>
<td></td>
<td>01</td>
<td>Two’s complement</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>Decrement the number by 1</td>
</tr>
<tr>
<td></td>
<td>11</td>
<td>One’s complement</td>
</tr>
</tbody>
</table>

For switch states 01, 10 and 11 you can assume that there is an implicit sign bit on the input signal which is always 0 (ie. your inputs range from 0000 to 0111). Your output for those switch settings will thus be a 4 bit number.

**Report**

a) Truth table of the design  
b) Boolean expressions that you derived from the truth table  
c) Circuit schematics  
d) One screen snapshot of the simulator outcome for the following input combinations:  
   X = 0 and (S0,S1) = {(0,0), (0,1), (1,0), (1,1)}  
   X = 3 and (S0,S1) = (0,1)

**Part 4: Selective decoder**

In this part you will be designing the decoding circuits for the encoder of part 3 to extract the original input value X. In order to identify the encoding scheme of the input, you can assume that the status of the selective switches (S0, S1) is available at the decoder side.
Report:

a) Truth table of the design
b) Boolean expressions that you derived from the truth table
c) Circuit schematics
d) One screen snapshot of the simulation outcome for the following input combinations:
   \[ Y = 0 \text{ and } (S0,S1) = \{(0,0), (0,1), (1,0), (1,1)\} \]
   \[ Y = 3 \text{ and } (S0,S1) = (0,1) \]

Part 5: Calculate delay

For the circuit shown, write answers to the following questions in your report:

a) What function does it implement? Show both truth table and logic equation.

b) Find the minimum and maximum delay from inputs \( (A, B, C) \) to the output \( Y \) of this circuit assuming the
   output is connected to another inverter. On resistance of NMOS transistor is \( R_n \), of PMOS is \( 2R_n \), and the
   gate capacitance of each transistor is \( C_g \).

c) Implement the same circuit using logic gates and simulate with Xilinx tools.
   Provide one screen snapshot of the simulator outcome for the following input combinations: \( (1, 0, 0) \).
   Measure the minimum and maximum delay. Provide a screen snapshot for the input combinations that give
   both min and max delay. Can you find what \( R_n \) and \( C_g \) are from these measurements? Why or why not?

d) Now simulate the same circuits with only NANDs and INV using Xilinx tools.
   Have minimum and maximum delays changed? Why or why not? Do your results from parts c and d match
   what we had discussed in class? Why or why not? Provide screen snapshots for minimum and maximum delay
   with those input combinations labeled.

Demonstration

You will need to demonstrate your project to lab TA in EBU3 3219. You may bring your own computer or use
the PCs available in the lab. The demonstration hours will be listed on the CSE 140L website by the next class.
The signup list will be on the door of EBU 3219.

Report Instruction

Your lab report should include:
- Title page: name, PID, title of lab and due date/time submitted.
- For all lab parts write your answers as requested above.

Grading

Lab assignment 1 accounts for 10% of the total four Lab assignments (Lab 1 =10%, Labs 2,3,4 together are 60%
of the total class grade). In this assignment, 30% of your grade will be from the demonstration and 70% will be
from the report.

*************** Good Luck! ***************