HPS, A New Microarchitecture: Rationale and Introduction

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Big Picture

• Three levels of parallelism
  • Big -- threads
  • Medium -- the compiler
  • Small -- hardware Their focus
Myopic, fine-grain Dataflow

- Restrict dataflow execution to an “active window”
- Feed it with a VN front end
- No more resource explosion
- Less parallelism
- At the mercy of the branch predictor
- Need a solution for memory ordering.
Components

• Merger -- integrate newly decoded instructions into the dataflow graph

• Register alias table -- map between logical register names and result buffer entries

• Node table -- Instruction scheduler. An entry for each instruction with ready bits.
Implementing HPS

- Node tables and register alias table are CAMs
- Long wires!
- Lots of area.
- Not very scalable.
Memory is hard

• Problem: Address and/or data are not known at merge time

• Solution
  • Build a memory alias table.
  • Insert mappings as address/data become known. Younger ops stall until then.