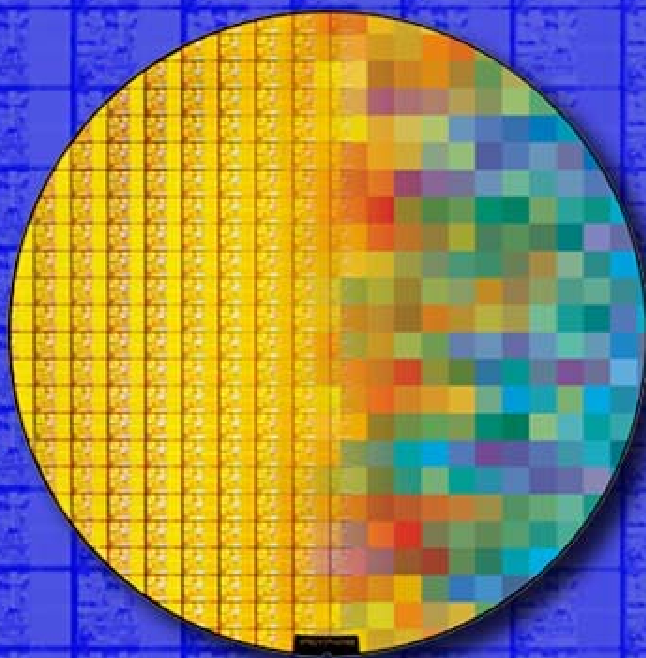
ITRS004



Optimization of Package Power Delivery and Power Removal Solutions to meet Platform level Challenges

Kaladhar Radhakrishnan
Michael J. Hill
Kemal Aygün
Chia-Pin Chiu
Gaurang Choksi

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Agenda

- Metrology for Platform Level Power Delivery Characterization
- New Power Delivery Architecture and Thermal Considerations for Multi-Core Servers
- Recent Advances in Package Power Delivery and Power Removal Solutions

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- **Metrology for Platform Level Power Delivery Characterization**
- **New Power Delivery Architecture and Thermal Considerations for Multi-Core Servers**
- **Recent Advances in Package Power Delivery and Power Removal Solutions**

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Enabling Platform Level Power Delivery Characterization

- The Power Delivery Network
- Time Domain Validation
- What is Z(f)?
- Measurement Setup
- Application Examples
- Status & Plans

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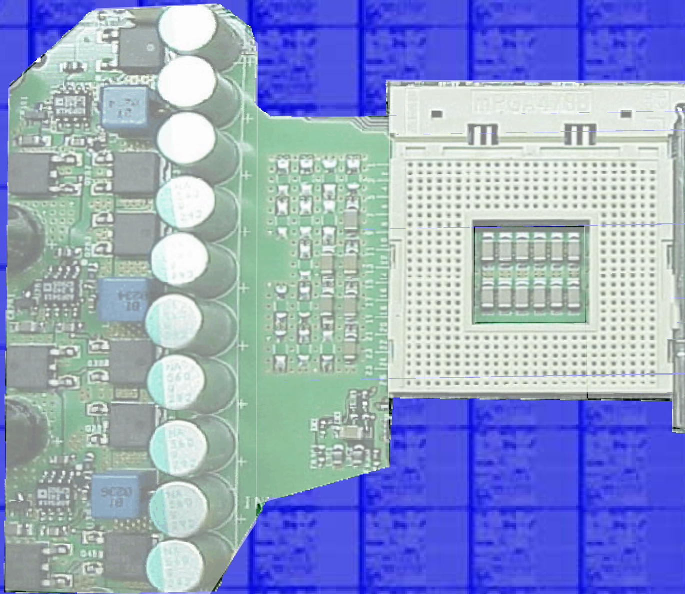
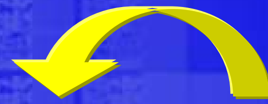
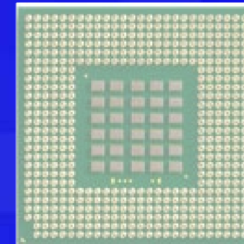
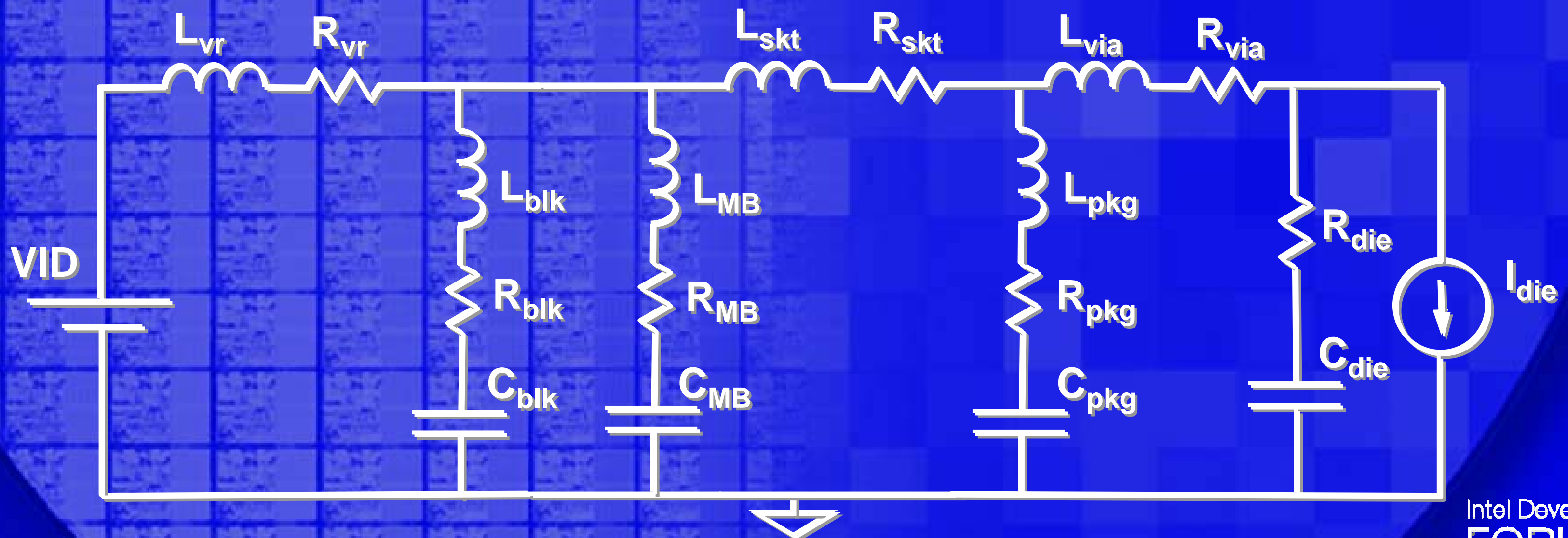
Typical Power Delivery Network









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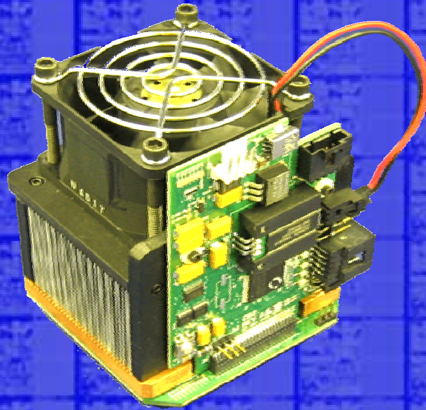
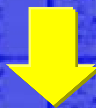
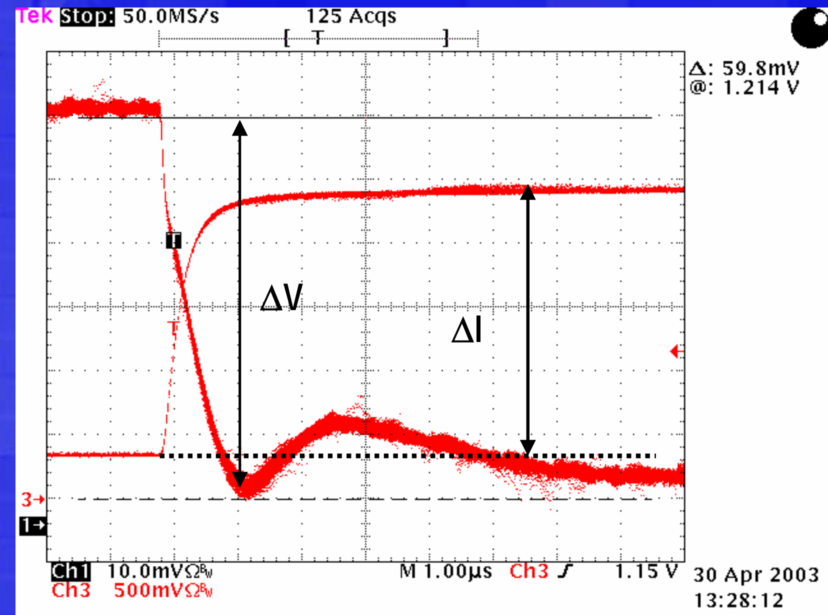
Time Domain Validation

Voltage Transient Test (VTT) Tool





Test Platform



Loadline = ΔV/ΔI

- VTT tool is used as CPU emulator
- Drawbacks with TD validation
  - VTT tool rise time different from that of processor
  - Not enough insight about the PD solution

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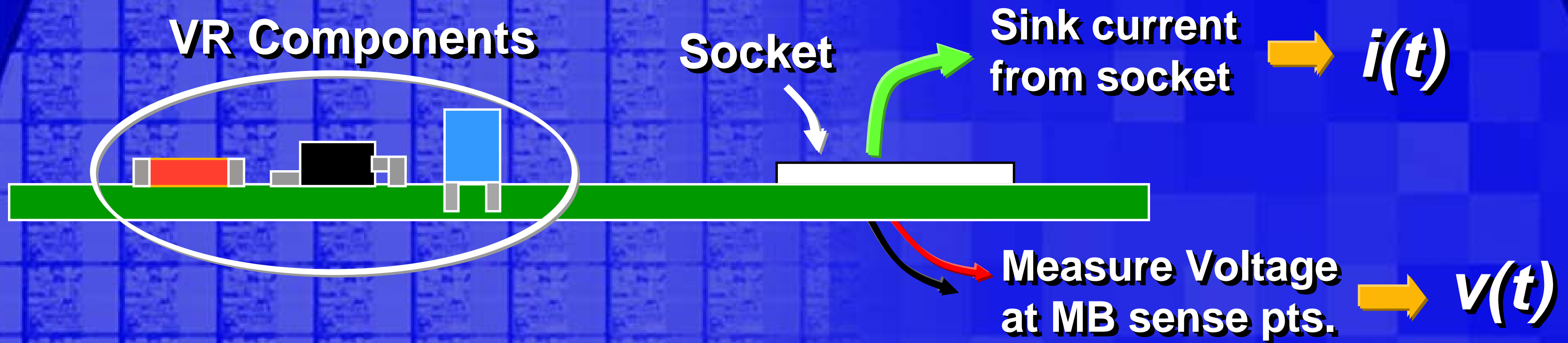
What is Z(f)?



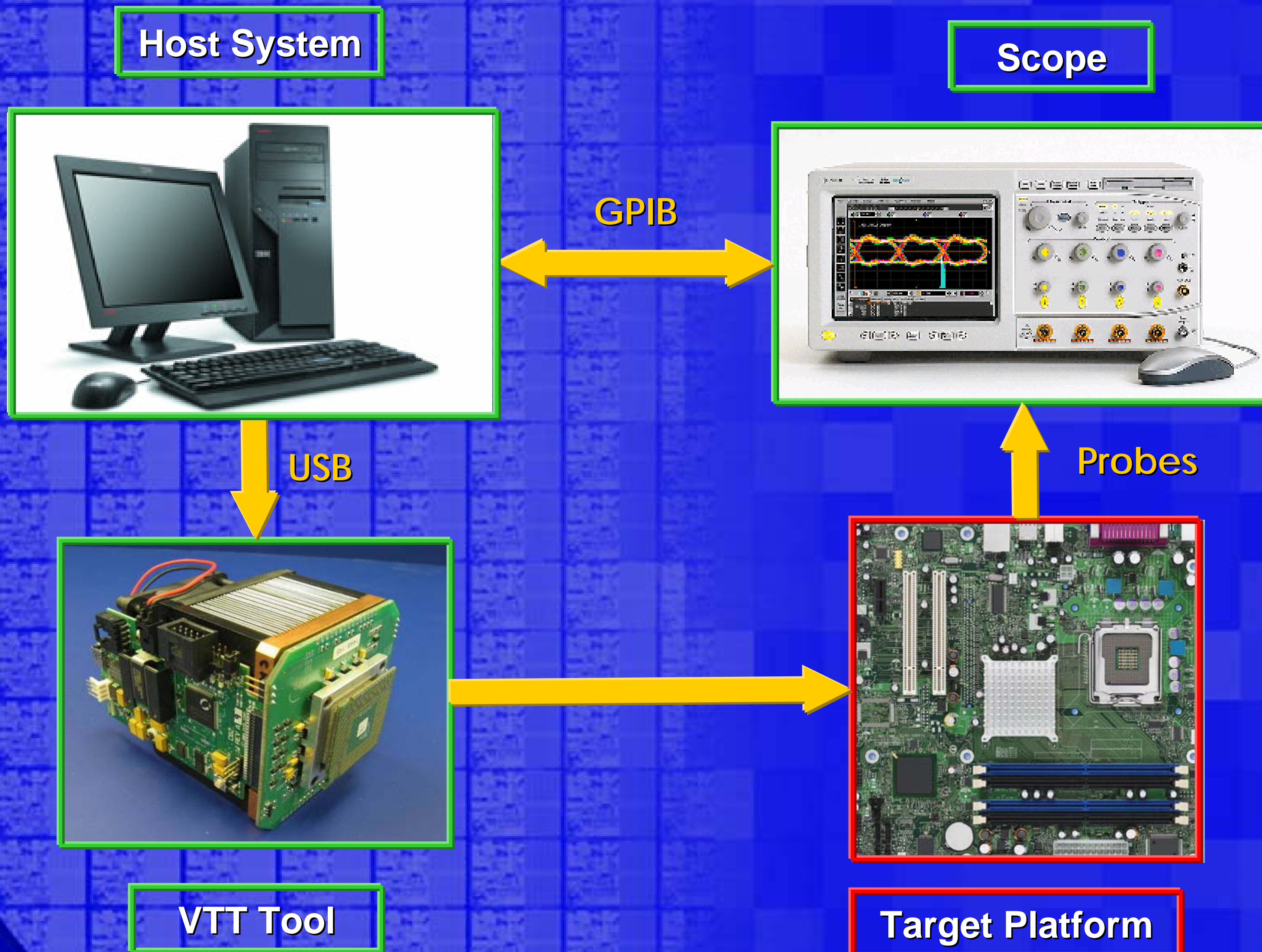
Fourier Transform can be used to determine frequency content of a time domain signal

$V(f) = FFT\{v(t)\}$

$I(f) = FFT\{i(t)\}$

$$Z(f)=V(f) / I(f)$$

Platform Z(f) – Measurement Setup



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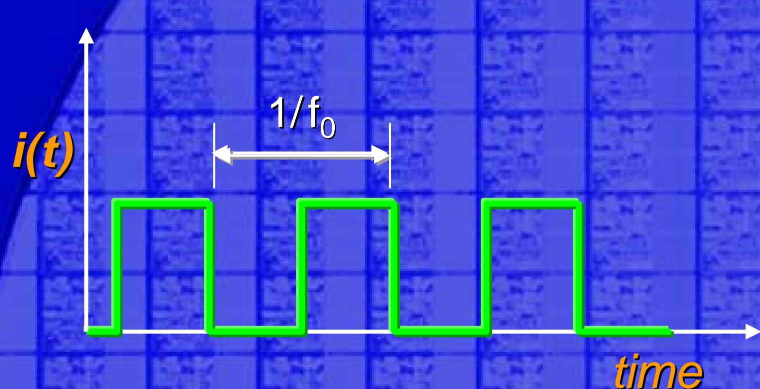
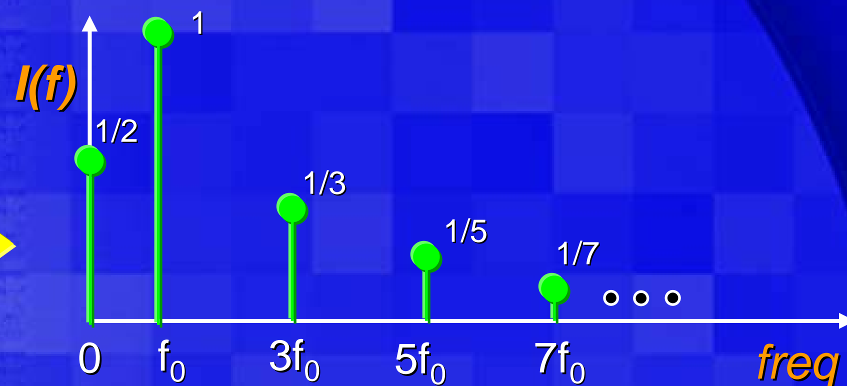
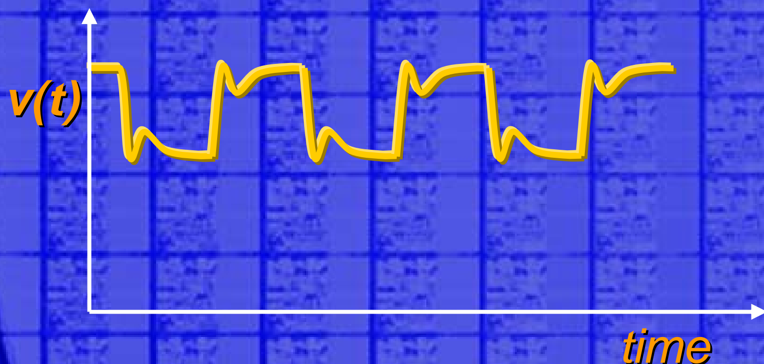
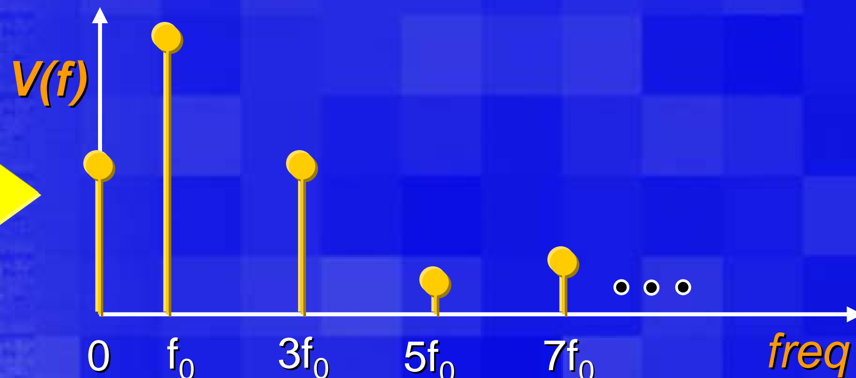
Time & Frequency Domains

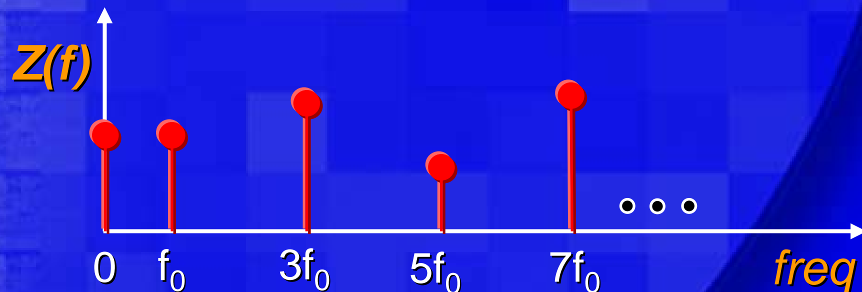








$$Z(f) = V(f) / I(f)$$



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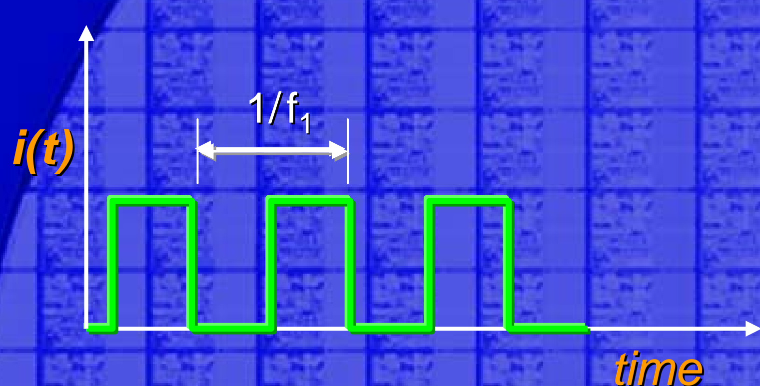
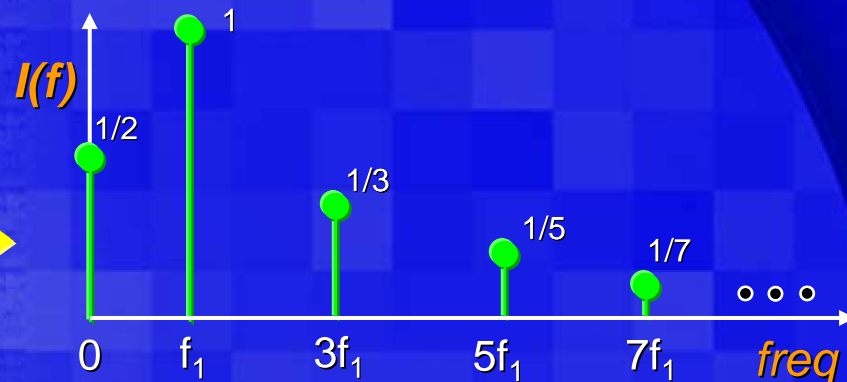
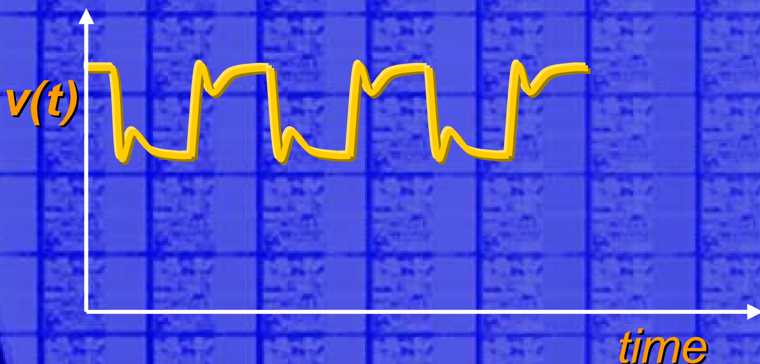
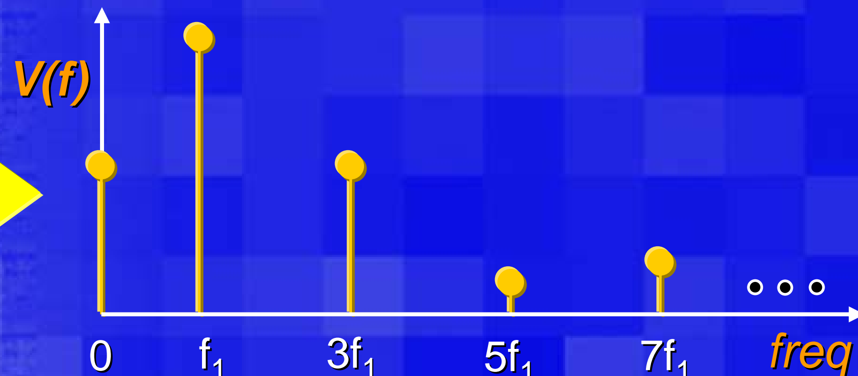
Time & Frequency Domains

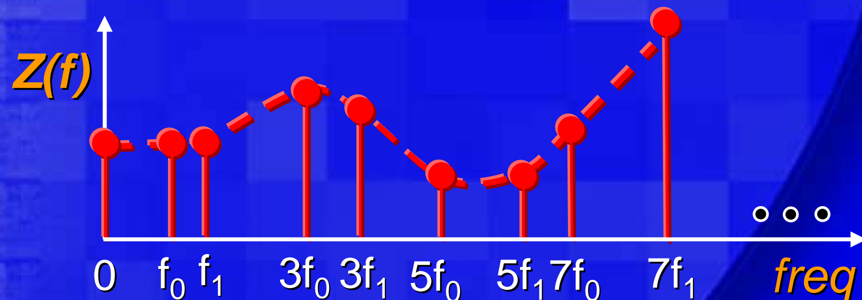








Sweep frequency to populate the data points on the impedance profile plot



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Automation

Station
Station #1
Station #2

Scope
AG5484(5)5A
TDS684C
initialize scope

Scope Settings
GPIB Address
7
Set
Vscale (mV/div)
50
Voffset (mV)
1300
Trig Level (mV)
700
Tigger Channel
Ch1 Ch3 Aux

COM port setting
4
DAC0
07FE
DAC1
0000

NFreq 100

1 0 60

Speci
Curre

actual f (kHz)
3,266.667
Imin (A) Imax (A) Imag (A)
0 60 60

Abort Measurement

313.06 u
9.9988 m
3.0625

intel.
Measuring impedance...
ATD Power Delivery
Exit

Platform Z(f) can be found in ~3-5 minutes

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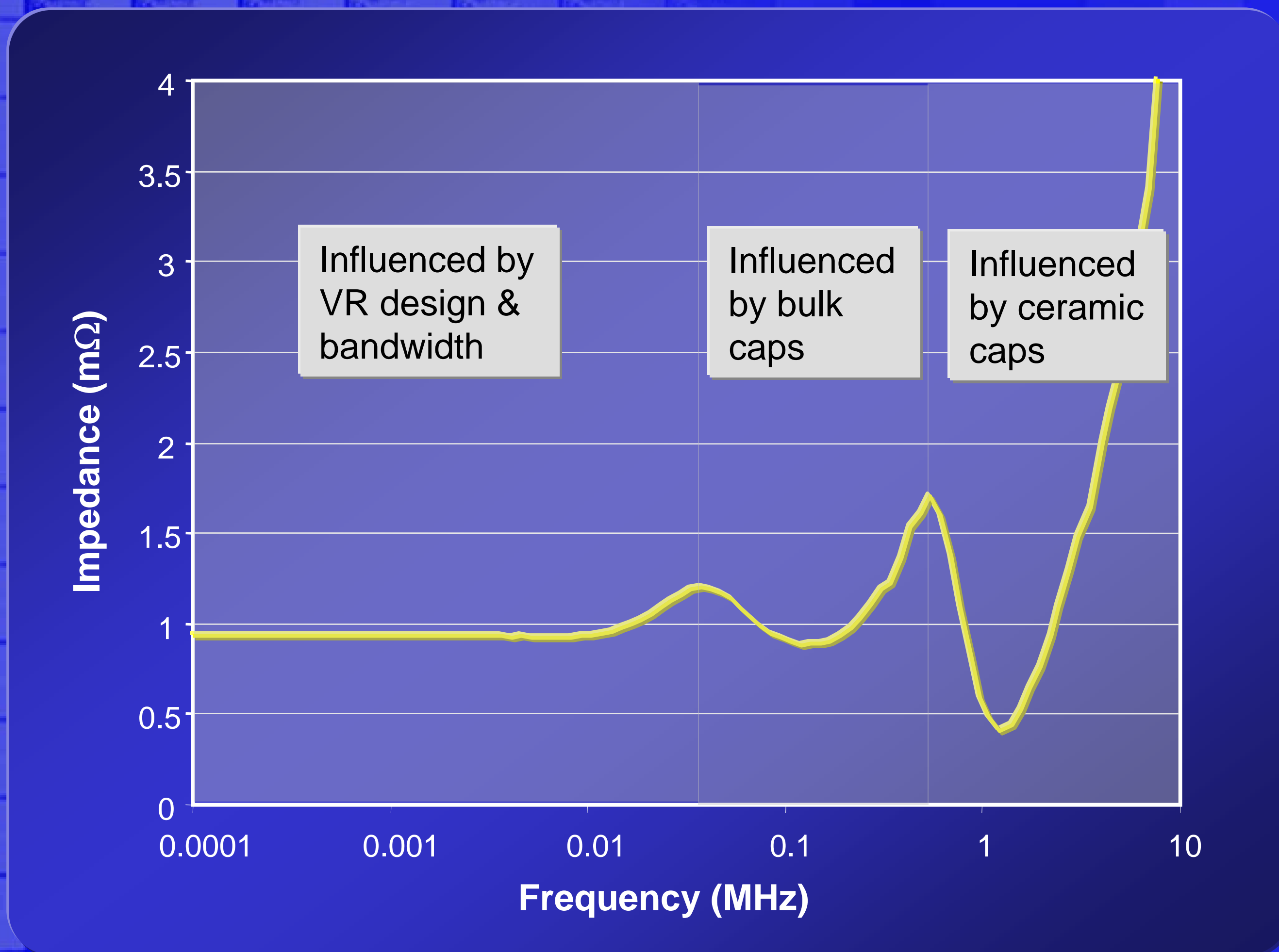
Typical Platform Z(f)



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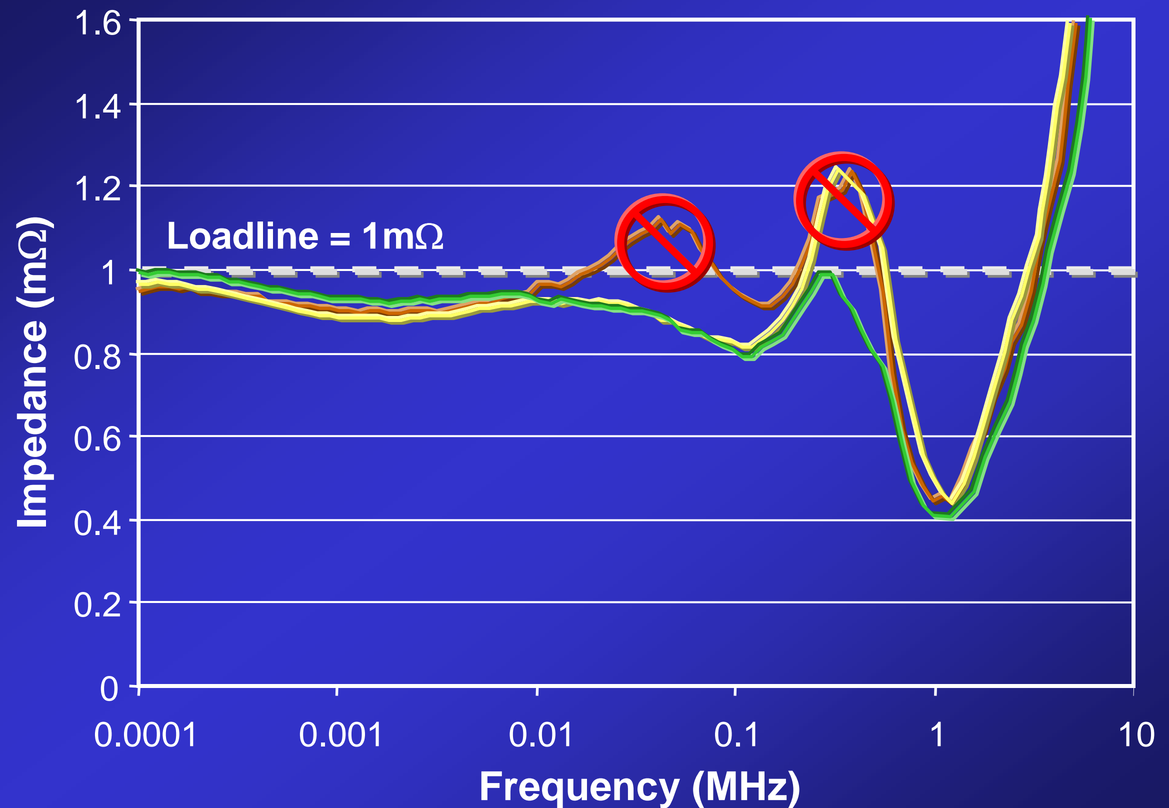
Application – LGA775 platform

10 x 560 uF Bulk Caps
12 x 22 uF MLCC Caps

10 x 820 uF Bulk Caps
12 x 22 uF MLCC Caps

10 x 820 uF Bulk Caps
16 x 22 uF MLCC Caps
2 x 47uF MLCC Caps



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Status & Plans for OEM Deployment

- Setup and plans demonstrated to OEMs
  - Aug 5 Intel Power Summit at Dupont, WA
- Customer version of the automation tool is currently being developed
  - Tool will be designed to support different measurement setups using multiple scopes
  - Automation tool will be made available to the OEMs along with the next release of the VTT tool

Summary

- Capability developed for fully automated platform impedance profile measurements
- Steps underway for deployment of measurement capability to OEMs

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Agenda

- Metrology for Platform Level Power Delivery Characterization
- New Power Delivery Architecture and Thermal Considerations for Multi-Core Servers
- Recent Advances in Package Power Delivery and Power Removal Solutions

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Novel PD Architecture and Thermal Considerations for Multi-Core Servers

- Itanium Server PD Architecture
- Xeon Server PD Architecture
- Motivation for new architecture
- New PD Scheme for Multi-Core Servers
- Thermal Considerations

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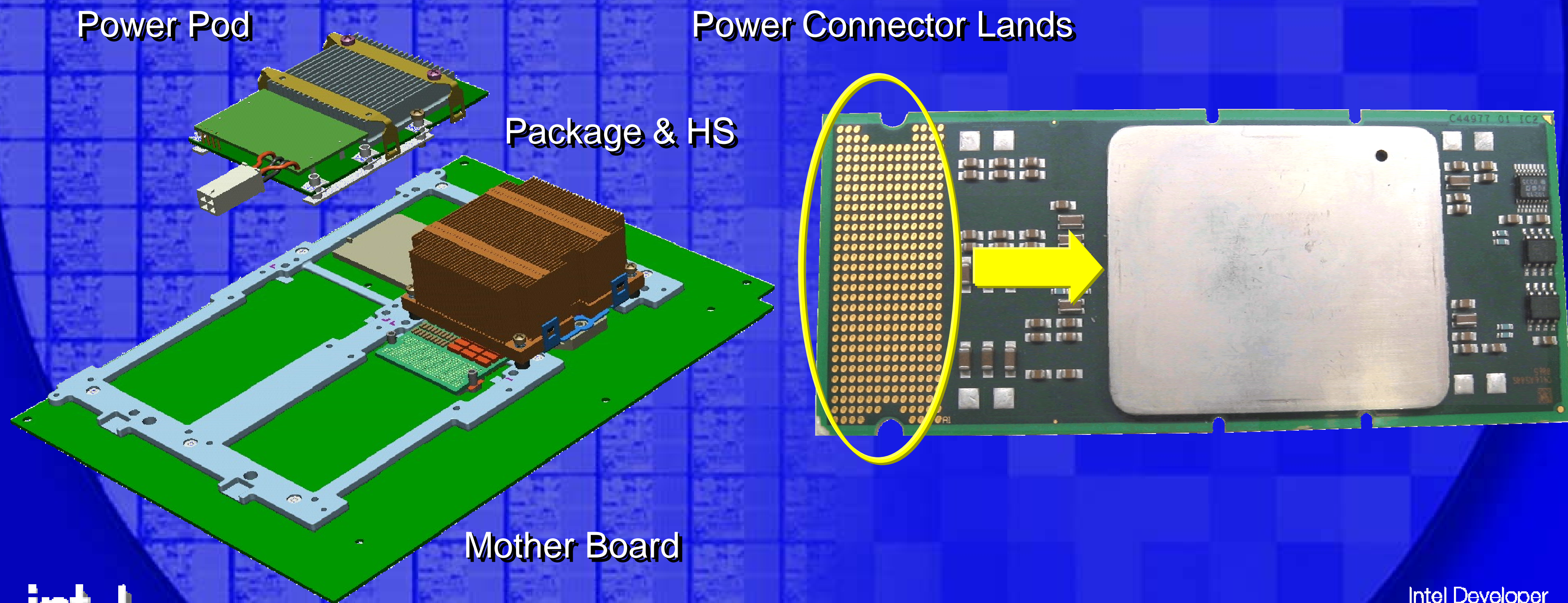
Itanium Server PD Architecture

- Power is supplied through a power pod
- Power is delivered through a topside power connector from one side of the package



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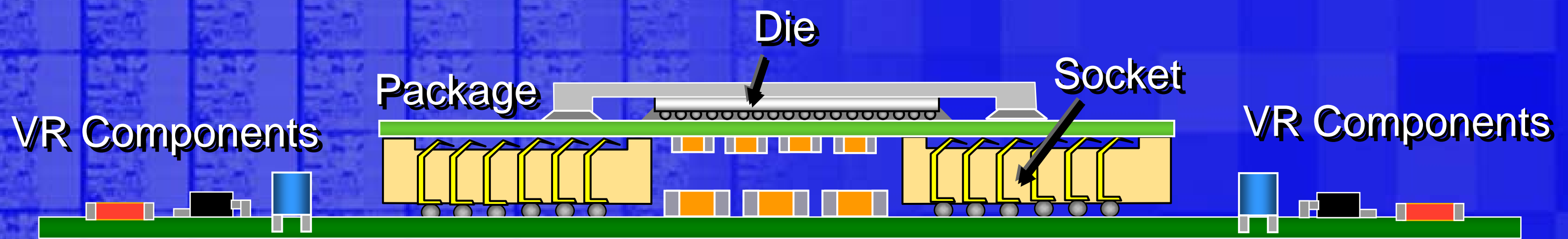
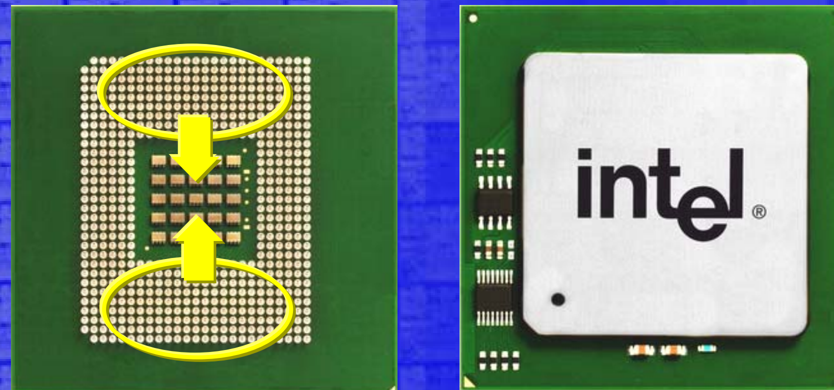
Xeon Server PD Architecture

- Power is supplied through pins on the socket
- Power is supplied from the voltage regulator through the pins from two sides on the package





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Motivation for New Architecture

- Power Delivery performance is limited with either PD architecture
- MB Real Estate for Power Delivery
- Opportunity for synergy between the Xeon and Itanium servers

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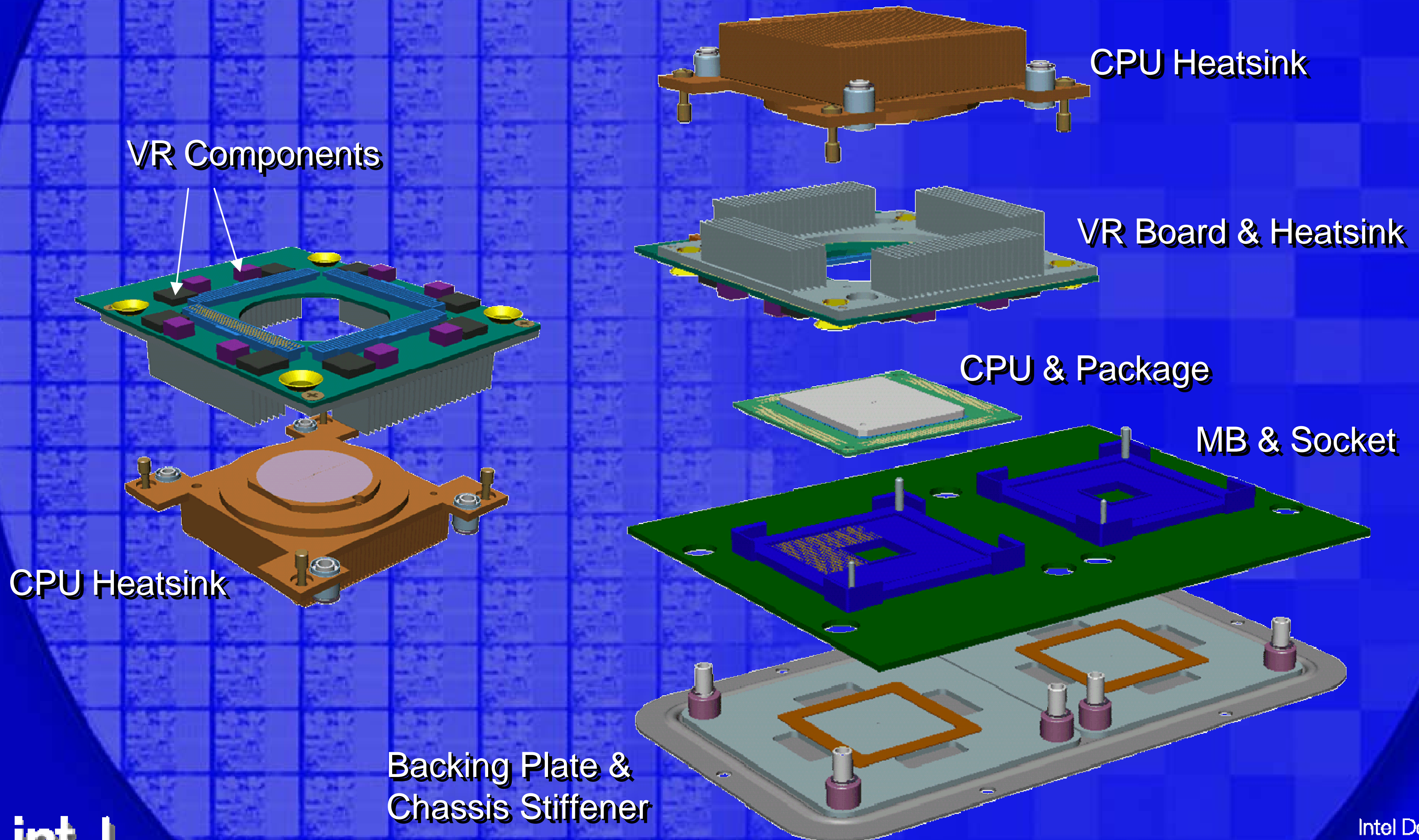
New Power Delivery Architecture



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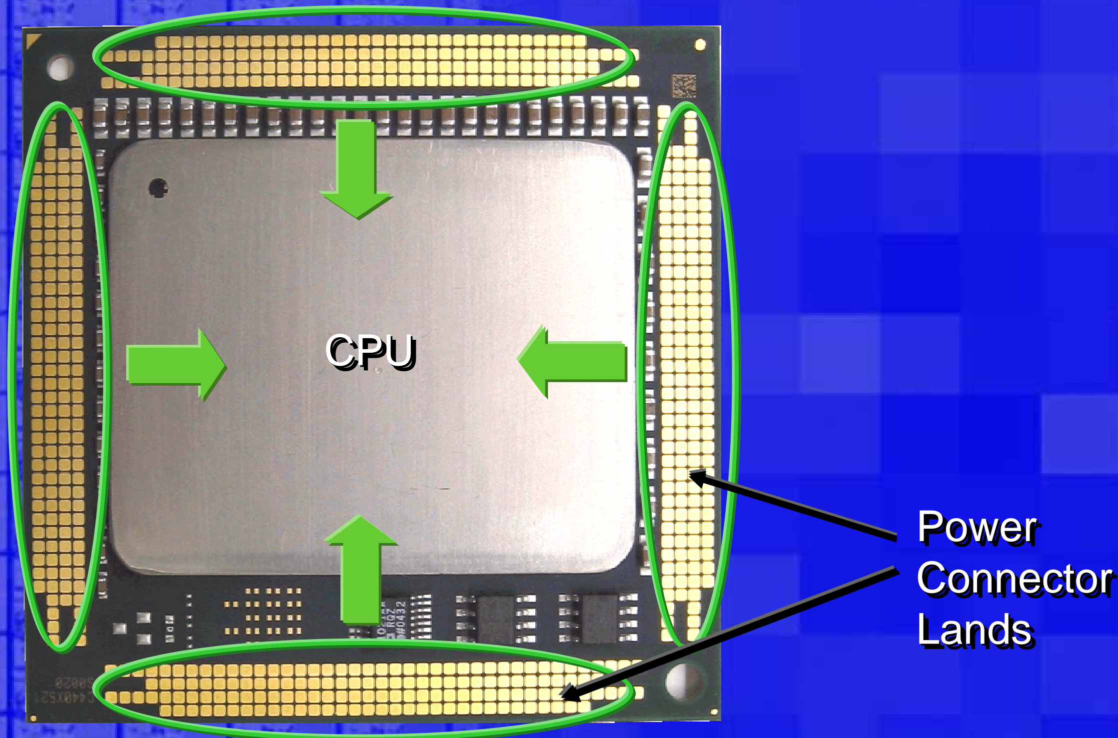
New Architecture – Package Details

- Four-sided power delivery scheme for improved performance
- Dedicated power connector is more scalable



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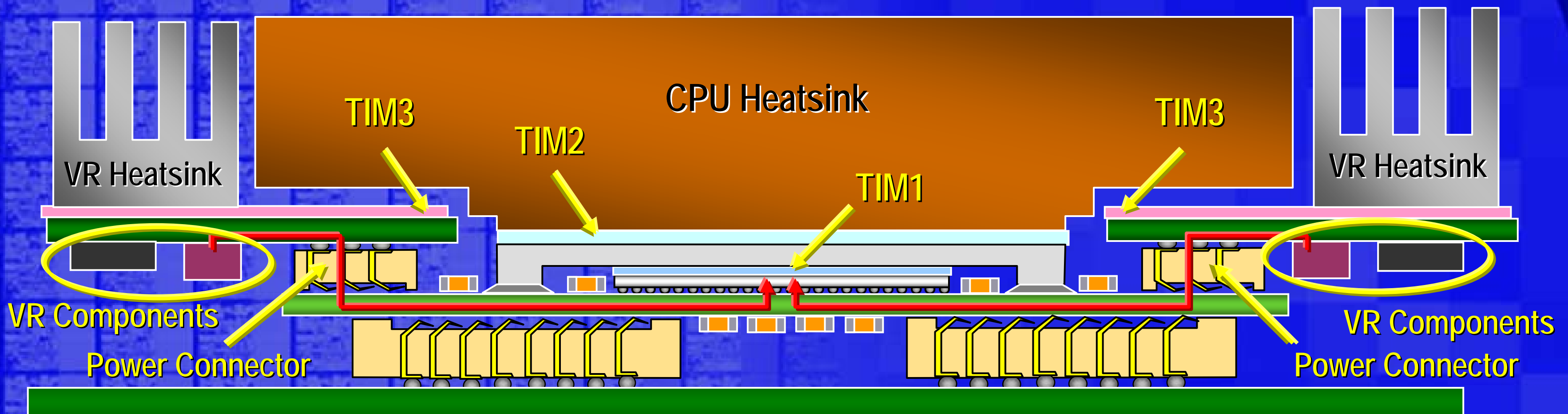
Cross-Section



- VR components moved to the VR board to free up MB real estate
- New TIM3 material introduced to cool VR components

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Thermal Considerations

- CPU Cooling
  - Increased die size due to multiple cores improves CPU cooling capacity
- VR Components
  - Increased power dissipation from the VR components due to the increasing current levels
  - New TIM3 material introduced to keep VR component temperature under spec
- Power Connector
  - Joule heating in the power delivery path can drive up power connector temperature
  - Need to contain maximum current through connector pins

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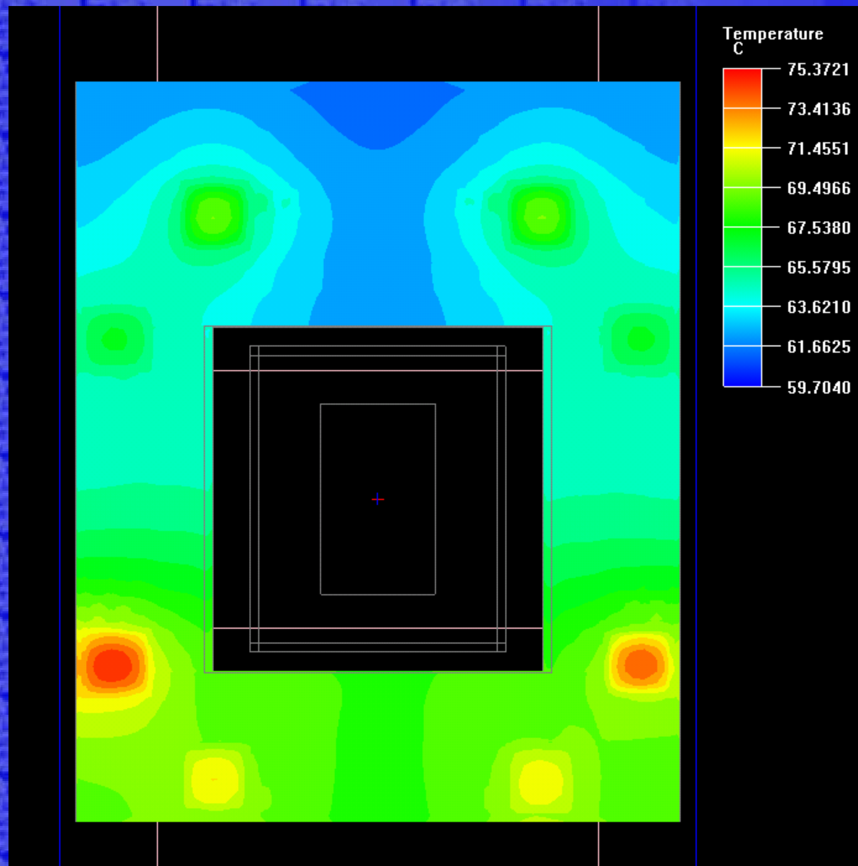
Thermal Analysis of the VR Board

- Global model to obtain temperature distribution across VR board



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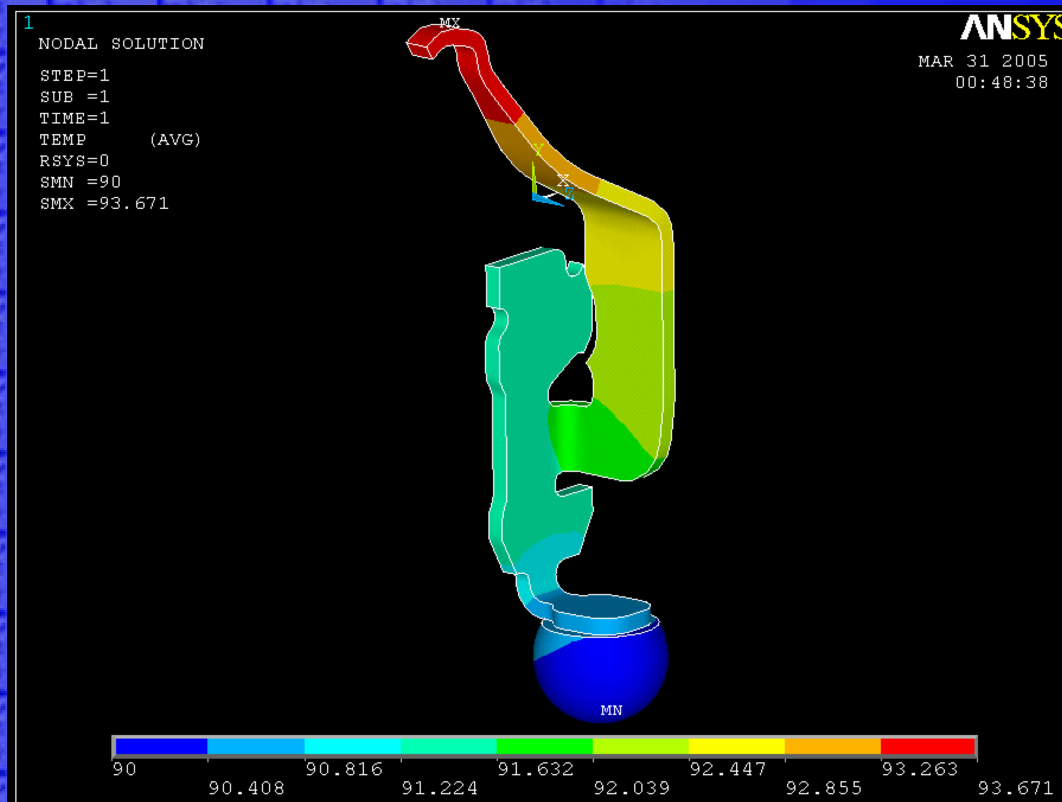
Thermal Analysis of the Connector

- Local model to estimate connector self-heating as a function of current through the pin



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Summary

- Novel PD architecture introduced for multi-core servers
  - 4 sided power delivery for better performance
  - Dedicated power connector makes the new architecture more scalable
- Unified platform strategy for Xeon and Itanium server products
- TIM3 material introduced to help keep VR and power connector temperature under spec

Agenda

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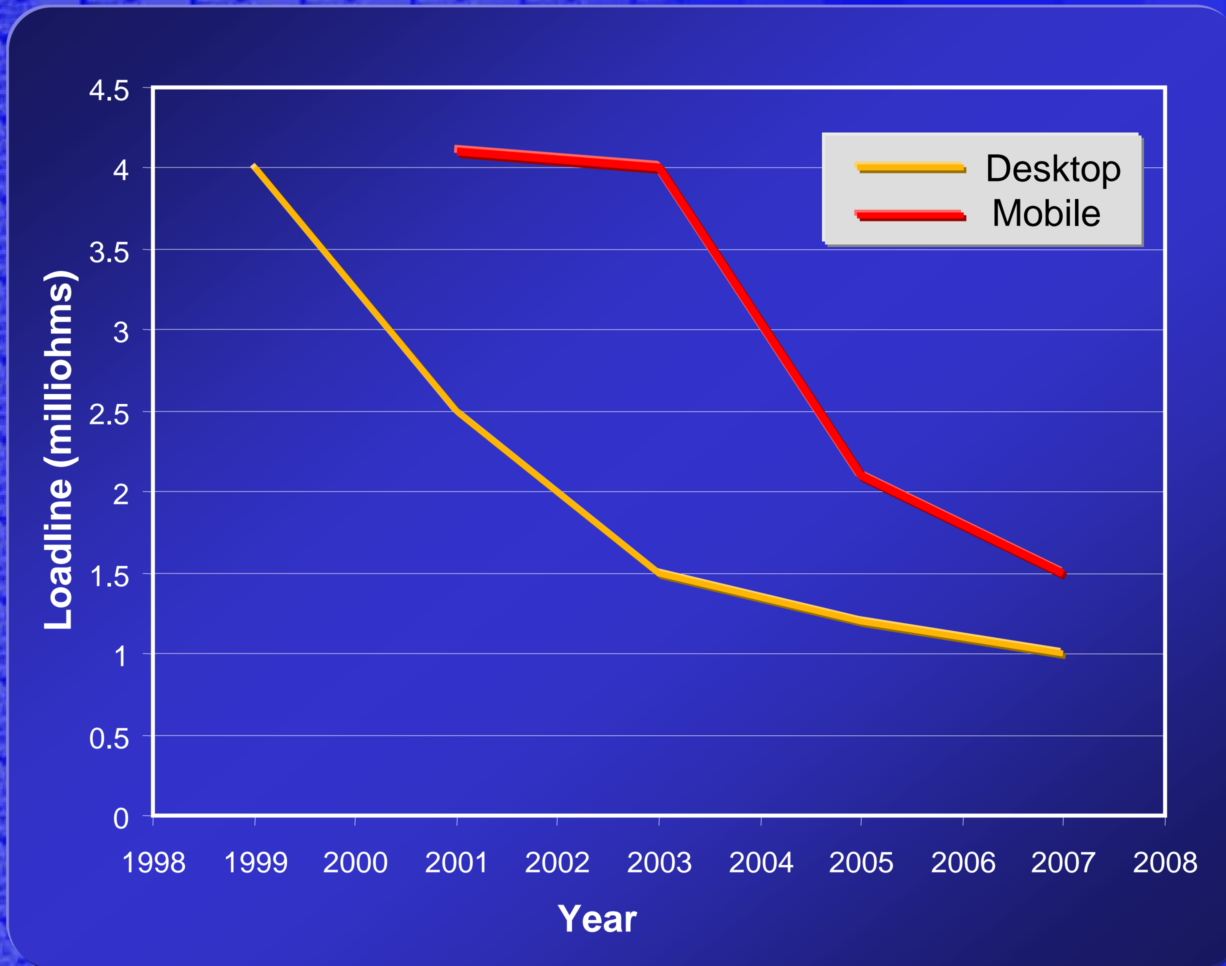
Advances in Package Power Delivery and Power Removal Solutions

- Desktop & Mobile Loadline Trends
- Evolution of Capacitors
- Advances in Socket Technology
- Package Technology Improvements
- Summary

Desktop & Mobile Loadline Trends



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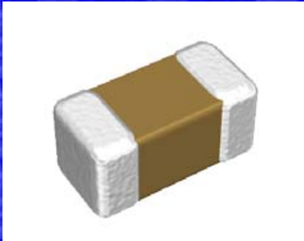
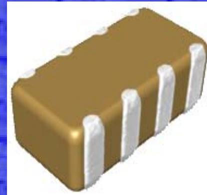
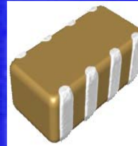
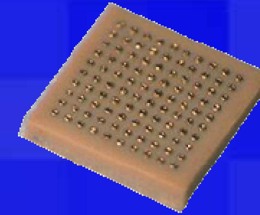
Capacitor Technology


0805 2T Capacitor


0805 IDC


0603 IDC


Array Capacitor

- Capacitor technology has evolved over the years
  - Transitioned from 2T capacitors to 0805 IDCs starting with processors in the 130 nm node
  - Processors in the 65 nm node have started using 0603 IDCs
  - Future generation processors could potentially use array capacitors if the technology warrants it

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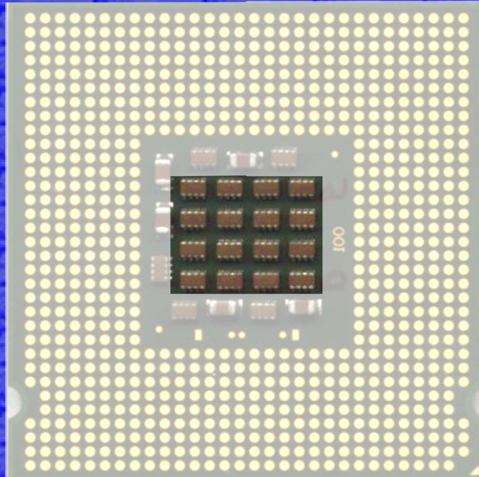
Capacitor Example

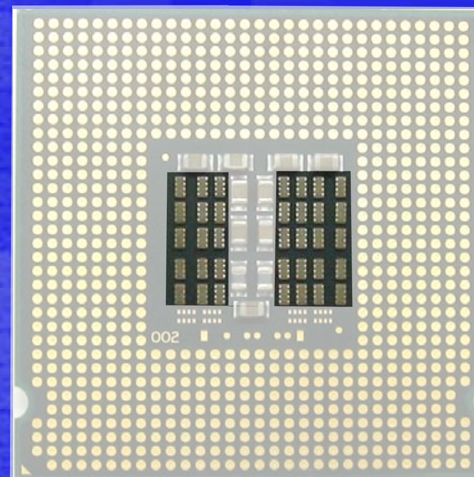
- Reducing body size drives up capacitor count

Single Core Processor



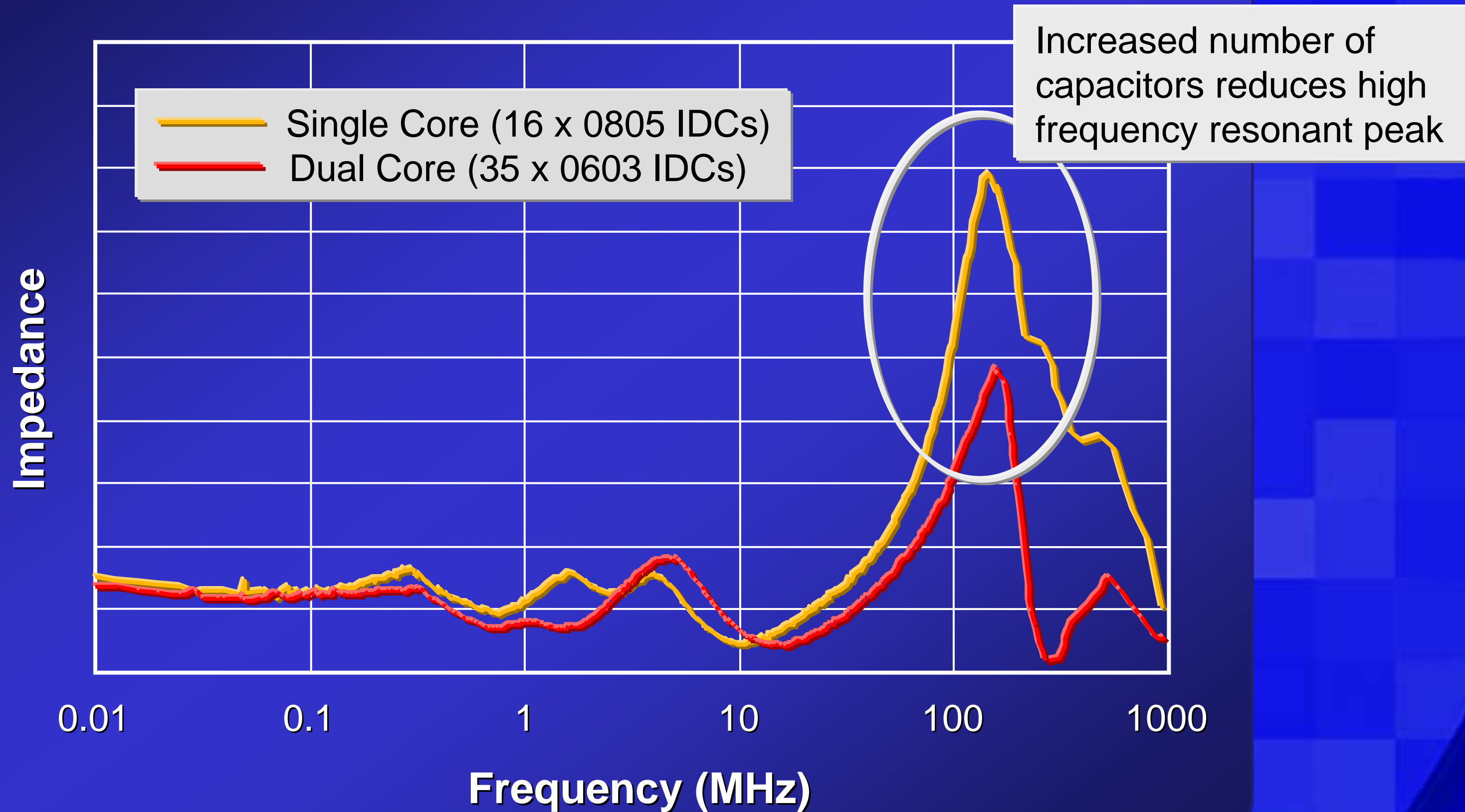
(16 x 0805 IDCs)

Dual Core Processor



(35 x 0603 IDCs)

Impedance Profile Comparison



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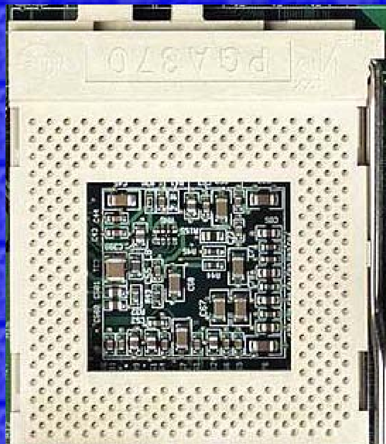
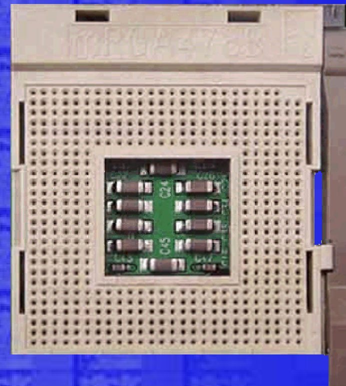
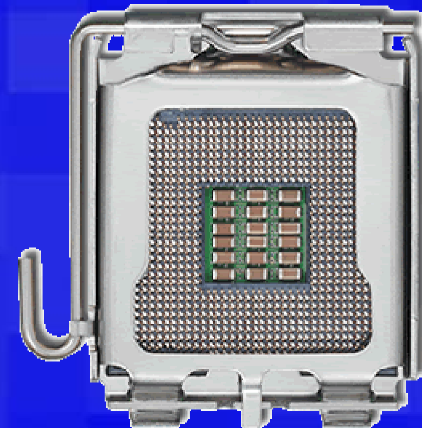
Socket Technology



Socket 370
49.5 x 49.5 mm



Socket 478
35 x 35 mm



Socket 775
37.5 x 37.5 mm

- **Improvement in socket technology has enabled us to scale the pitch and fit more pins for a given area**

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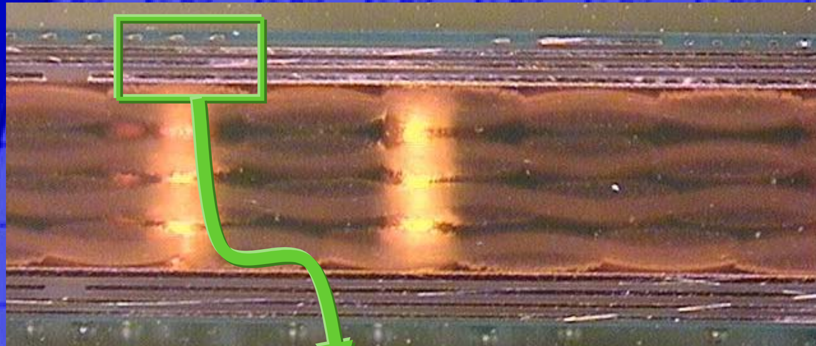
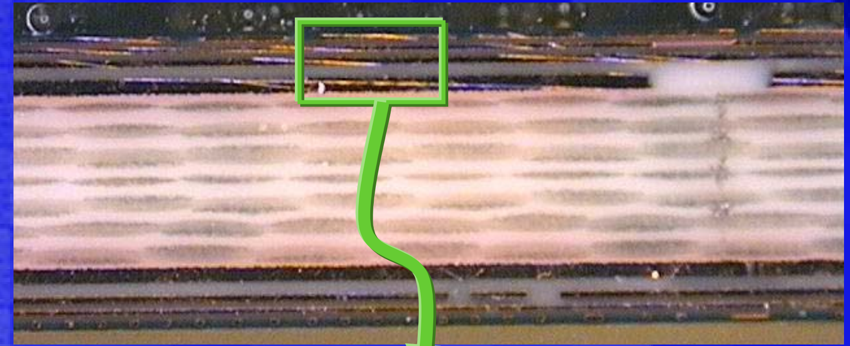
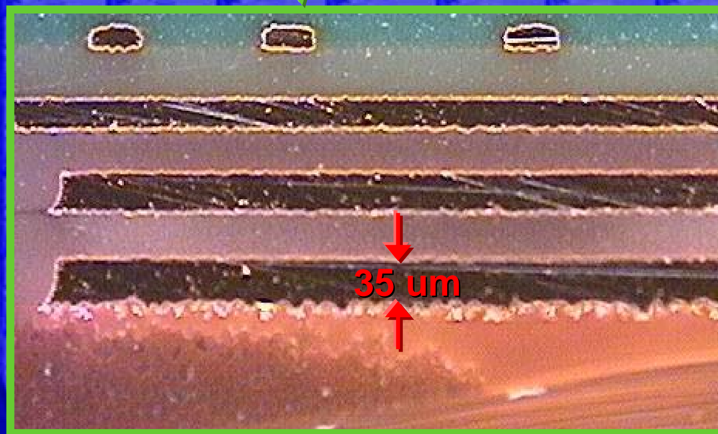
Package Resistance

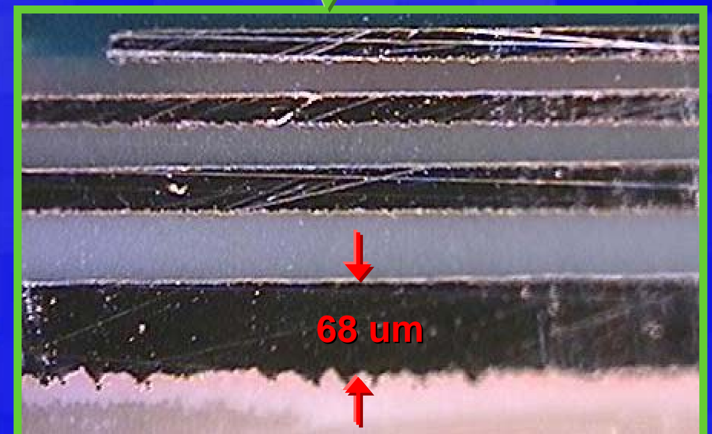
90nm Processor Package

65nm Processor Package









- Packages for the 65nm processors have increased copper in the core layers to reduce resistance

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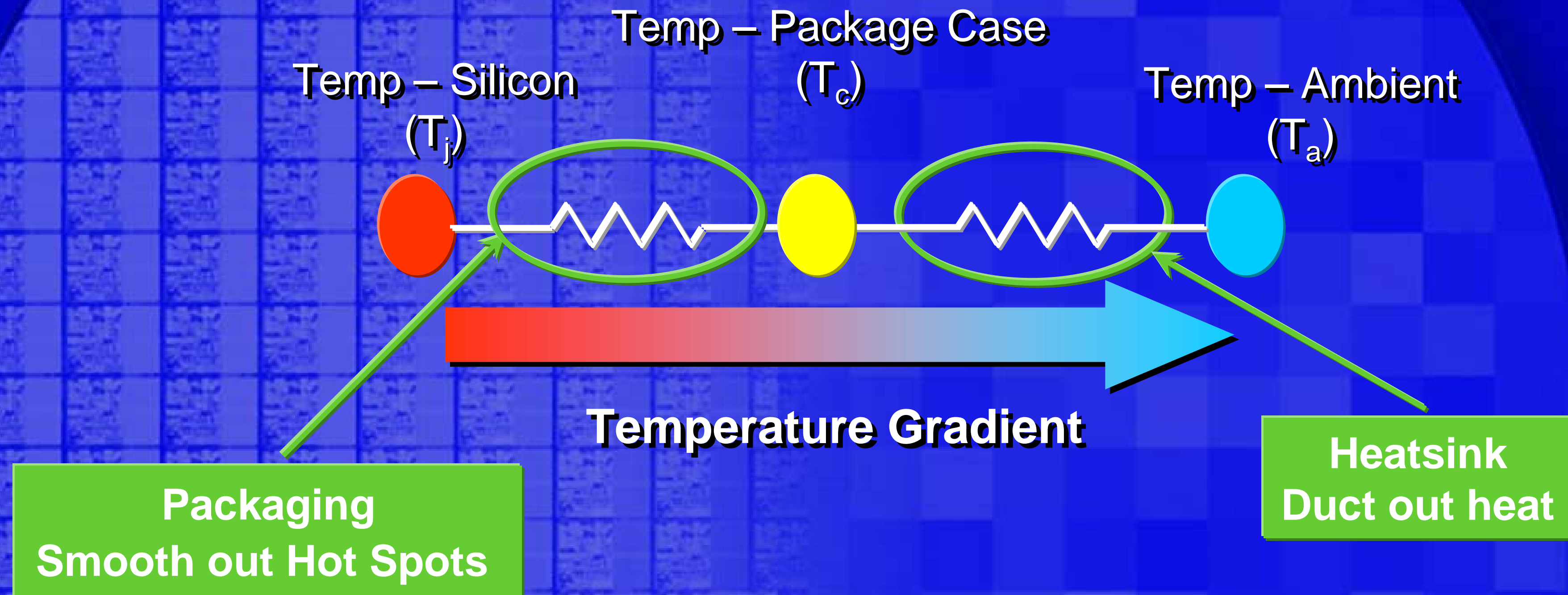
Power Removal Strategies



- **Packaging Strategy**
  - Hot spot mitigation
  - Reduction in thermal resistance (bulk & interface)
- **Heat Sink Strategy**
  - Material & Geometry Optimization
  - Cost effective manufacturability

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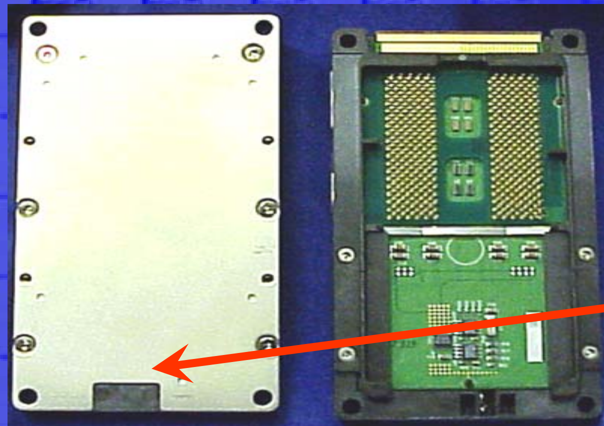
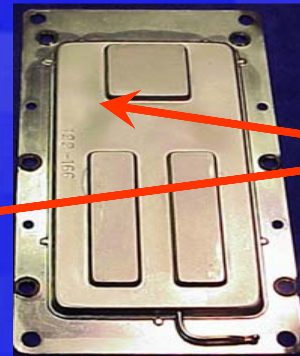
Hot Spot mitigation

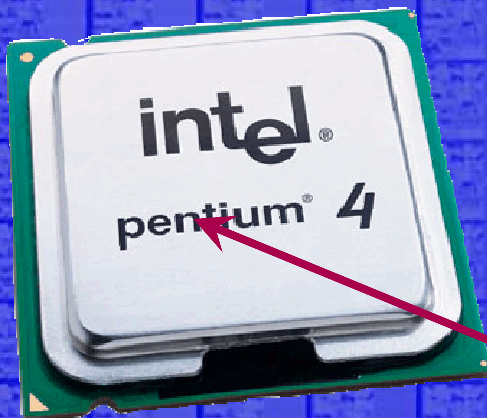
Example: Itanium

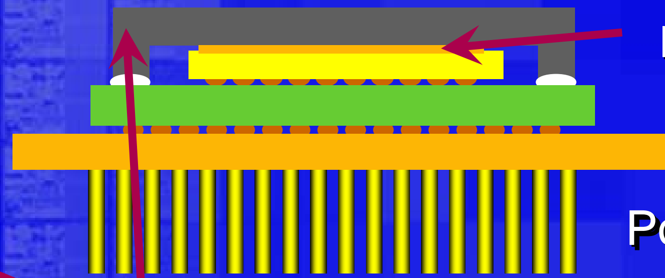




Integrated heat pipe

Example: Pentium 4





High conductivity Interface Material

Polymer -> Solder

Integrated Heat Spreader

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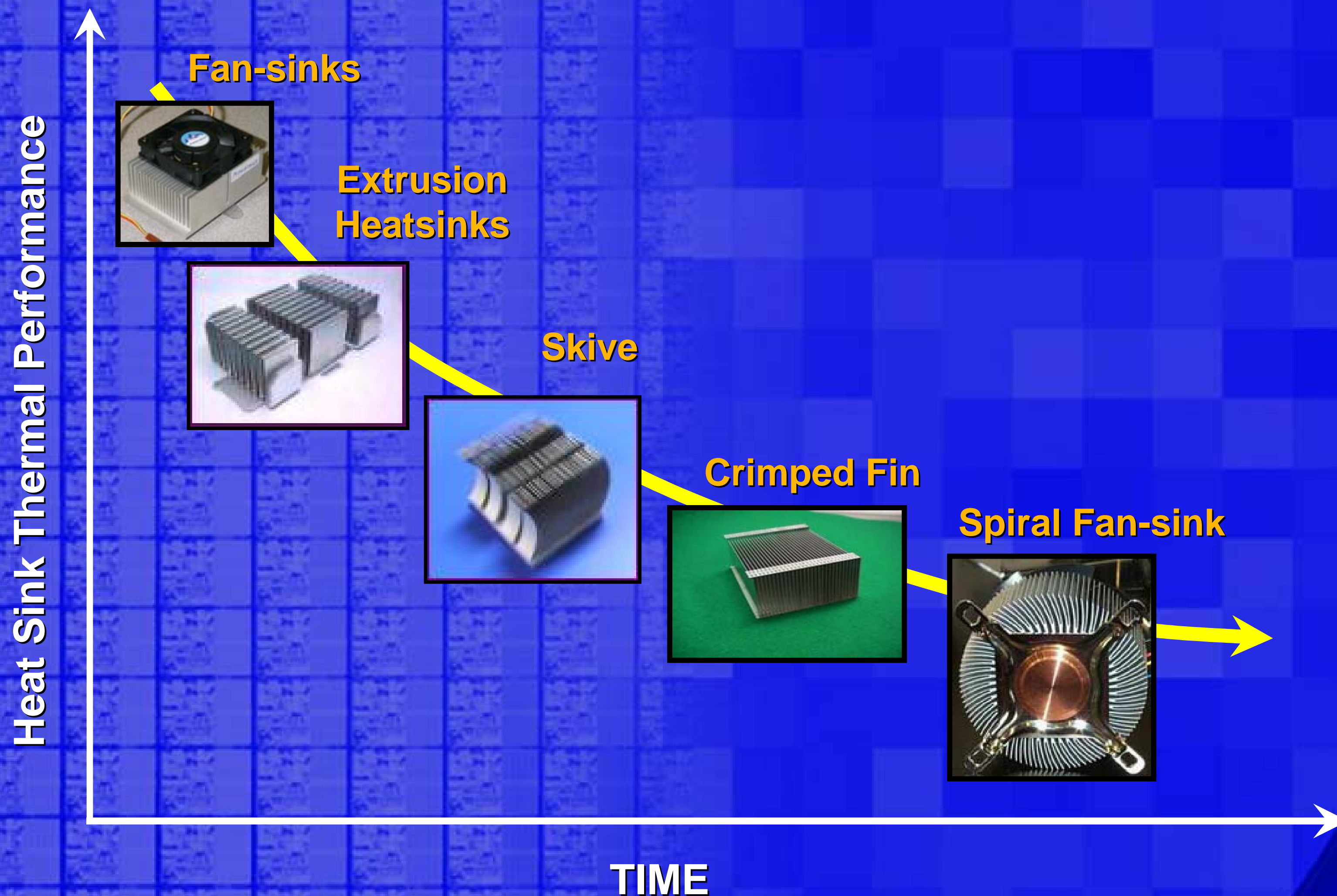
Heat Sink Technology



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Summary

- The power delivery impedance target has been shrinking steadily over the years
- Capacitor technology has been steadily improving to address high frequency noise
- Improvements in socket and package technology help reduce DC resistance
- Use of the heat spreader and better TIM material have reduce package thermal resistance
- Heat sink technology has been improving to enhance cooling capability without driving up cost

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Please fill out the Session Evaluation Form.

Thank You!

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