Optimization of Package Power Delivery and Power Removal Solutions to meet Platform level Challenges

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Agenda

- Metrology for Platform Level Power Delivery Characterization
- New Power Delivery Architecture and Thermal Considerations for Multi-Core Servers
- Recent Advances in Package Power Delivery and Power Removal Solutions
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- Metrology for Platform Level Power Delivery Characterization
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Enabling Platform Level Power Delivery Characterization

- The Power Delivery Network
- Time Domain Validation
- What is Z(f)?
- Measurement Setup
- Application Examples
- Status & Plans
Typical Power Delivery Network

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Time Domain Validation

Voltage Transient Test (VTT) Tool

Test Platform

Loadline = \Delta V/\Delta I

- VTT tool is used as CPU emulator
- Drawbacks with TD validation
  - VTT tool rise time different from that of processor
  - Not enough insight about the PD solution
What is $Z(f)$?

VR Components

Socket

Sink current from socket

Measure Voltage at MB sense pts.

$V(t)$

$i(t)$

$V(f) = \text{FFT}\{v(t)\}$

$I(f) = \text{FFT}\{i(t)\}$

$Z(f) = V(f) / I(f)$

Fourier Transform can be used to determine frequency content of a time domain signal.
Platform Z(f) – Measurement Setup

- Host System
- Scope
- USB
- GPIB
- Probes
- VTT Tool
- Target Platform

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**Time & Frequency Domains**

- **$i(t)$**
  - 1 cycle over 1 period, $1/f_0$

- **$v(t)$**
  - 1 cycle over 1 period

- **$I(f)$**
  - Frequency domain of $i(t)$
  - Points at $f_0$, $3f_0$, $5f_0$, $7f_0$, ...

- **$V(f)$**
  - Frequency domain of $v(t)$
  - Points at $f_0$, $3f_0$, $5f_0$, $7f_0$, ...

- **$Z(f) = V(f) / I(f)$**

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Time & Frequency Domains

Sweep frequency to populate the data points on the impedance profile plot

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Automation

Platform Z(f) can be found in ~3-5 minutes
Typical Platform \( Z(f) \)

Impedance (mΩ) vs. Frequency (MHz)

- Influenced by VR design & bandwidth
- Influenced by bulk caps
- Influenced by ceramic caps

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Application – LGA775 platform

Bulk Caps

MLCC Caps

10 x 560 uF Bulk Caps
12 x 22 uF MLCC Caps
10 x 820 uF Bulk Caps
12 x 22 uF MLCC Caps
10 x 820 uF Bulk Caps
16 x 22 uF MLCC Caps
2 x 47uF MLCC Caps

Impedance (mΩ)

Frequency (MHz)

Loadline = 1mΩ

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Status & Plans for OEM Deployment

• Setup and plans demonstrated to OEMs
  – Aug 5 Intel Power Summit at Dupont, WA

• Customer version of the automation tool is currently being developed
  – Tool will be designed to support different measurement setups using multiple scopes
  – Automation tool will be made available to the OEMs along with the next release of the VTT tool
Summary

- Capability developed for fully automated platform impedance profile measurements
- Steps underway for deployment of measurement capability to OEMs
Agenda

- Metrology for Platform Level Power Delivery Characterization
- **New Power Delivery Architecture and Thermal Considerations for Multi-Core Servers**
- Recent Advances in Package Power Delivery and Power Removal Solutions
Novel PD Architecture and Thermal Considerations for Multi-Core Servers

- Itanium Server PD Architecture
- Xeon Server PD Architecture
- Motivation for new architecture
- New PD Scheme for Multi-Core Servers
- Thermal Considerations
Itanium Server PD Architecture

- Power is supplied through a power pod
- Power is delivered through a topside power connector from one side of the package
Xeon Server PD Architecture

- Power is supplied through pins on the socket
- Power is supplied from the voltage regulator through the pins from two sides on the package

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Motivation for New Architecture

- Power Delivery performance is limited with either PD architecture
- MB Real Estate for Power Delivery
- Opportunity for synergy between the Xeon and Itanium servers
New Power Delivery Architecture

- New Power Delivery Architecture
- CPU & Package
- VR Board & Heatsink
- CPU Heatsink
- VR Components
- Backing Plate & Chassis Stiffener
- MB & Socket

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New Architecture – Package Details

- Four-sided power delivery scheme for improved performance
- Dedicated power connector is more scalable
- VR components moved to the VR board to free up MB real estate
- New TIM3 material introduced to cool VR components
Thermal Considerations

- **CPU Cooling**
  - Increased die size due to multiple cores improves CPU cooling capacity

- **VR Components**
  - Increased power dissipation from the VR components due to the increasing current levels
  - New TIM3 material introduced to keep VR component temperature under spec

- **Power Connector**
  - Joule heating in the power delivery path can drive up power connector temperature
  - Need to contain maximum current through connector pins
Thermal Analysis of the VR Board

- Global model to obtain temperature distribution across VR board
Thermal Analysis of the Connector

- Local model to estimate connector self-heating as a function of current through the pin
Summary

- Novel PD architecture introduced for multi-core servers
  - 4 sided power delivery for better performance
  - Dedicated power connector makes the new architecture more scalable
- Unified platform strategy for Xeon and Itanium server products
- TIM3 material introduced to help keep VR and power connector temperature under spec
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Advances in Package Power Delivery and Power Removal Solutions

- Desktop & Mobile Loadline Trends
- Evolution of Capacitors
- Advances in Socket Technology
- Package Technology Improvements
- Summary
Desktop & Mobile Loadline Trends

- Loadline (milliohms) vs. Year (1998-2008)
- Yellow line represents Desktop, red line represents Mobile

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Capacitor Technology

- Capacitor technology has evolved over the years
  - Transitioned from 2T capacitors to 0805 IDCs starting with processors in the 130 nm node
  - Processors in the 65 nm node have started using 0603 IDCs
  - Future generation processors could potentially use array capacitors if the technology warrants it
Capacitor Example

- Reducing body size drives up capacitor count

Single Core Processor

(16 x 0805 IDCs)

Dual Core Processor

(35 x 0603 IDCs)
Impedance Profile Comparison

Increased number of capacitors reduces high frequency resonant peak

Impedance vs. Frequency

- Single Core (16 x 0805 IDCs)
- Dual Core (35 x 0603 IDCs)
Improvement in socket technology has enabled us to scale the pitch and fit more pins for a given area.
Packages for the 65nm processors have increased copper in the core layers to reduce resistance.
Power Removal Strategies

- **Packaging Strategy**
  - Hot spot mitigation
  - Reduction in thermal resistance (bulk & interface)

- **Heat Sink Strategy**
  - Material & Geometry Optimization
  - Cost effective manufacturability
Hot Spot mitigation

Example: Itanium

Example: Pentium 4

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Heat Sink Technology

Heat Sink Thermal Performance vs. TIME

- Fan-sinks
- Extrusion Heatsinks
- Skive
- Crimped Fin
- Spiral Fan-sink

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Summary

- The power delivery impedance target has been shrinking steadily over the years
- Capacitor technology has been steadily improving to address high frequency noise
- Improvements in socket and package technology help reduce DC resistance
- Use of the heat spreader and better TIM material have reduce package thermal resistance
- Heat sink technology has been improving to enhance cooling capability without driving up cost
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