Microprocessor Packaging

The Key Link in the Chain

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Intel Corporation

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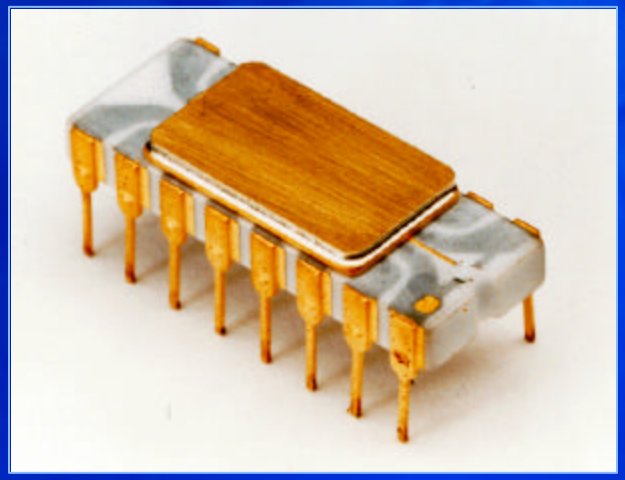
Microprocessors



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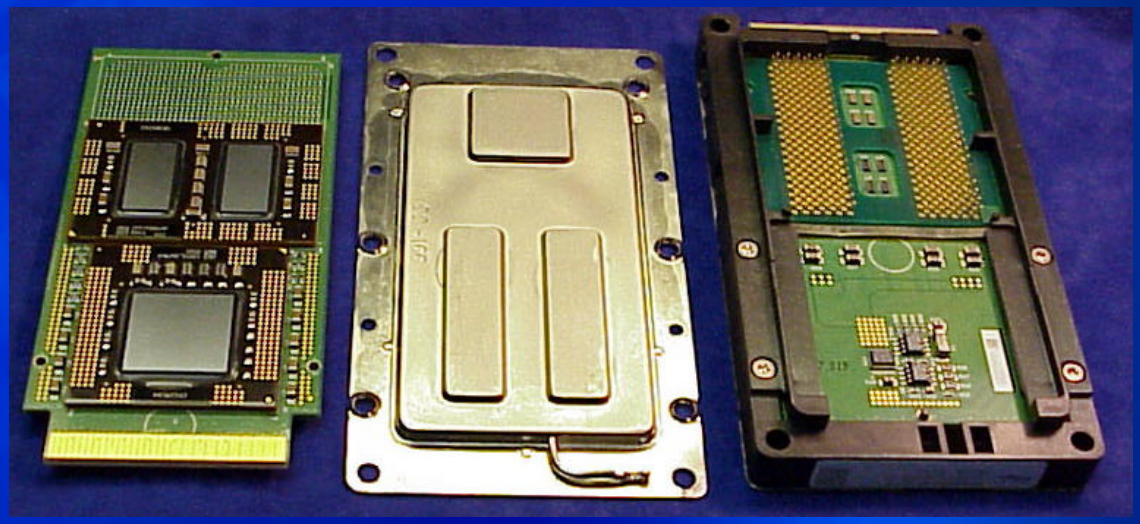

2001

Global Packaging R&D

Virtual ATD

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Main R&D facility in Chandler, AZ

Computing needs driving complexity

First to introduce organic in mainstream CPUs

First to introduce flip chip in mainstream CPUs

Intel 486™ Processor

25 MHz → 1.0+ GHz

Ceramic To Organic

Wire-bond To Flip Chip

Looking ahead …

Complexity and Challenges to support Moore's Law

1. Silicon to package interconnect
2. Within package interconnect
3. Power management
4. Adding more functionality

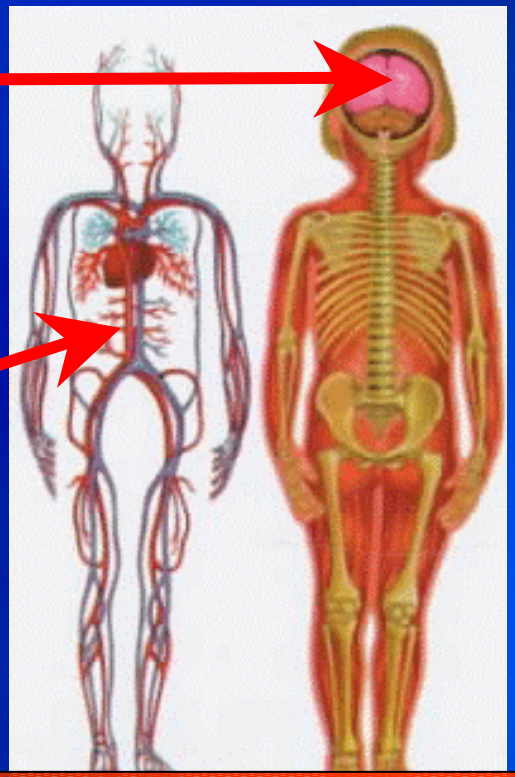
Goal : Bring technology innovation into High volume manufacturing at a LOW COST

Silicon & Package Relationship

Anatomy 101

Silicon Processor:
The "brain" of the computer (generates instructions)

Packaging:
The rest of the body (Communicates instructions to the outside world, adds protection)



No Package = No Product !
Great Packaging = Great Products !!

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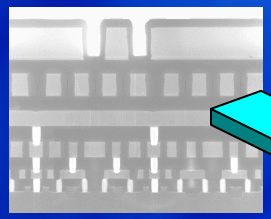
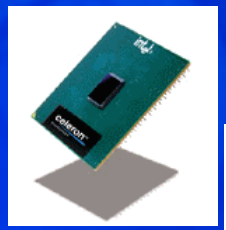
The Key Link in the Chain



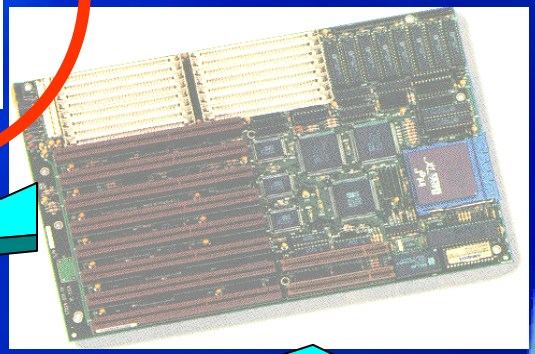
Transistor-to-Transistor
Ckt Blk to Ckt Blk

Chip-to-Package



Key Link in the chain

Package-
to-Board



Board-to-System

Opportunity

Innovative, efficient, high performance, low-cost packages are a significant competitive advantage

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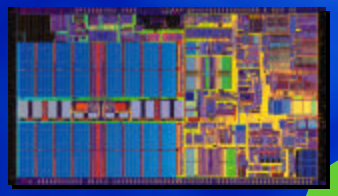
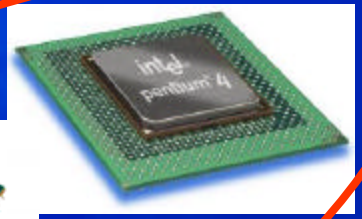
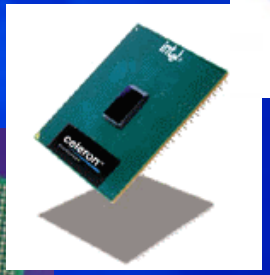
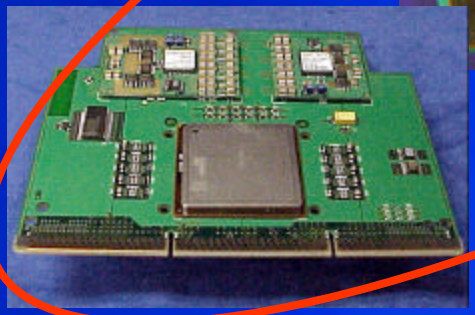
Example – Enabling Custom solutions

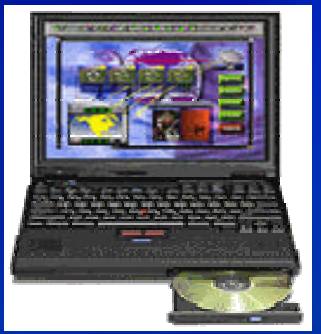


Silicon Enabler



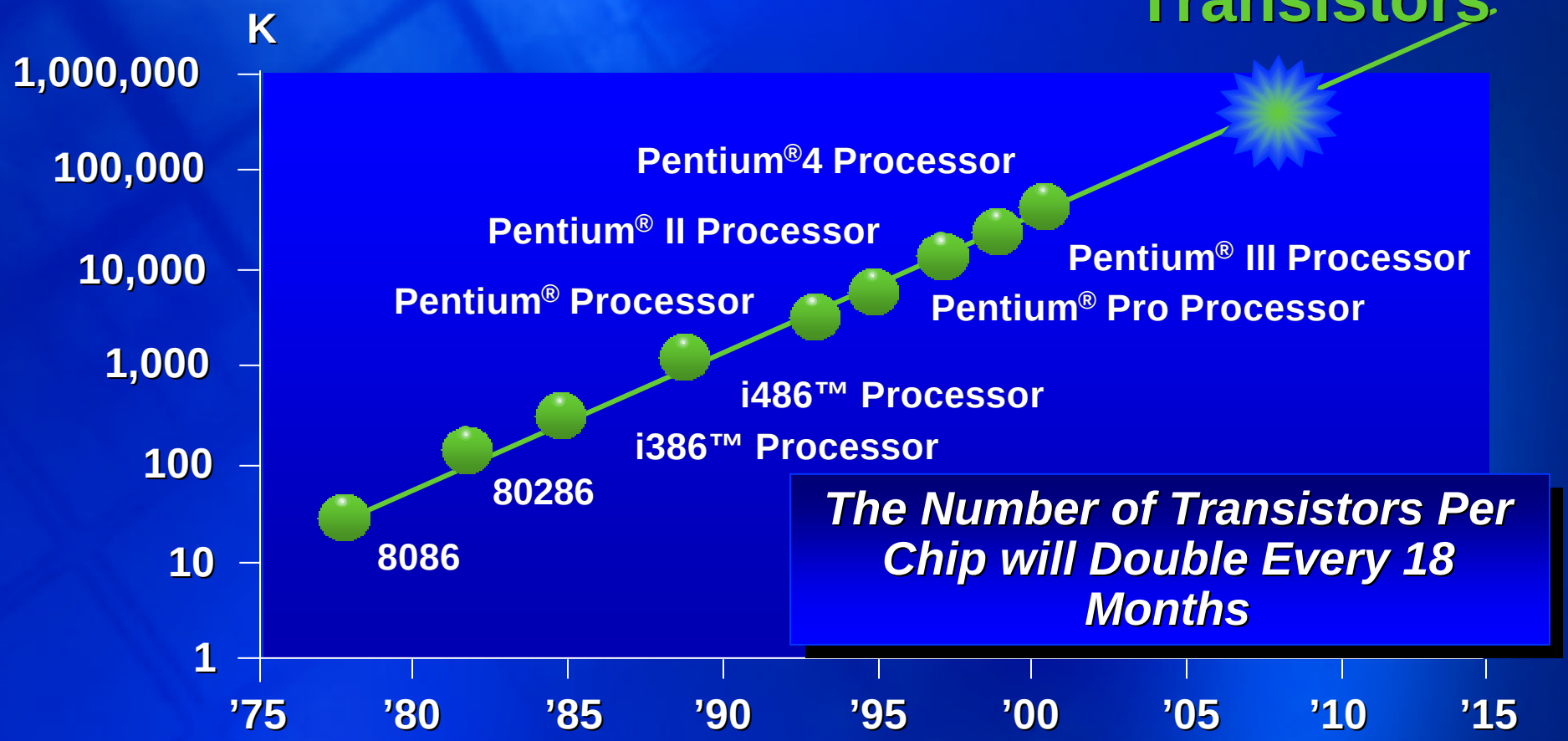






Value Add : custom solutions based on market segment

Breaking Barriers to Moore's Law



The Number of Transistors Per Chip will Double Every 18 Months

Source: Intel

Integrated Packaging + Silicon Technology development is essential

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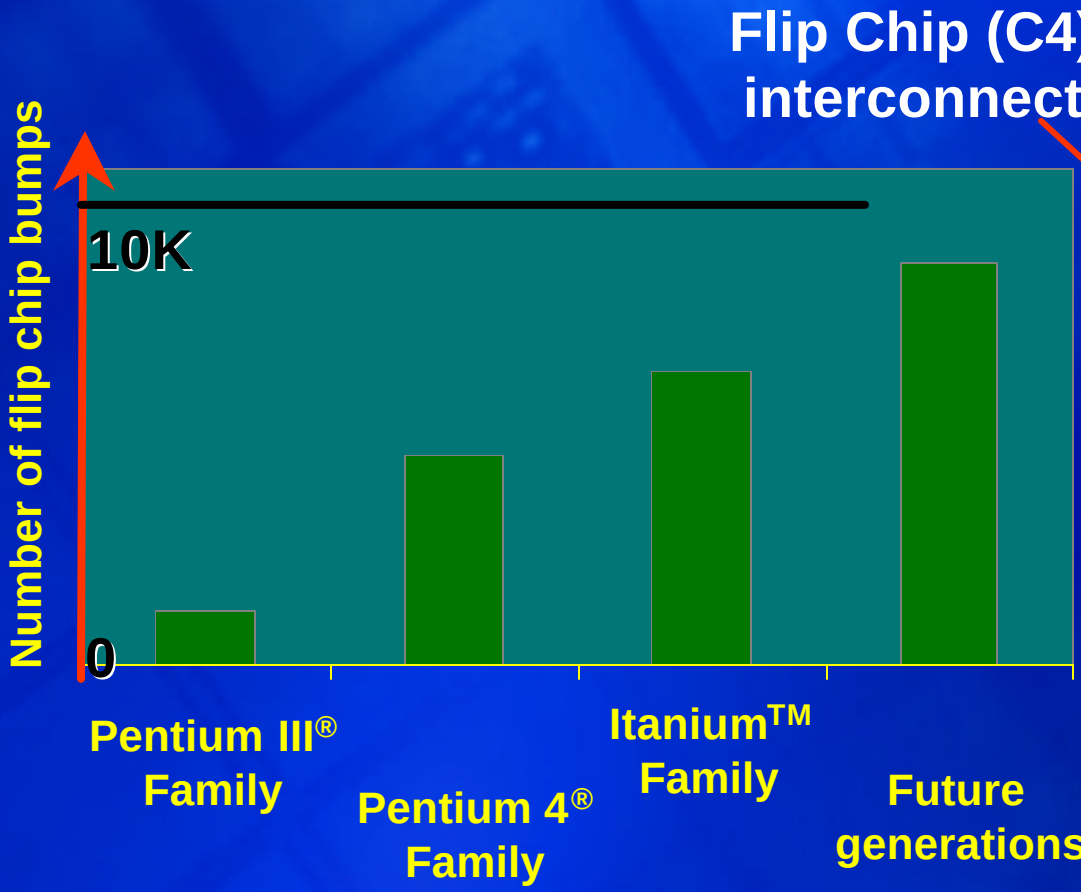
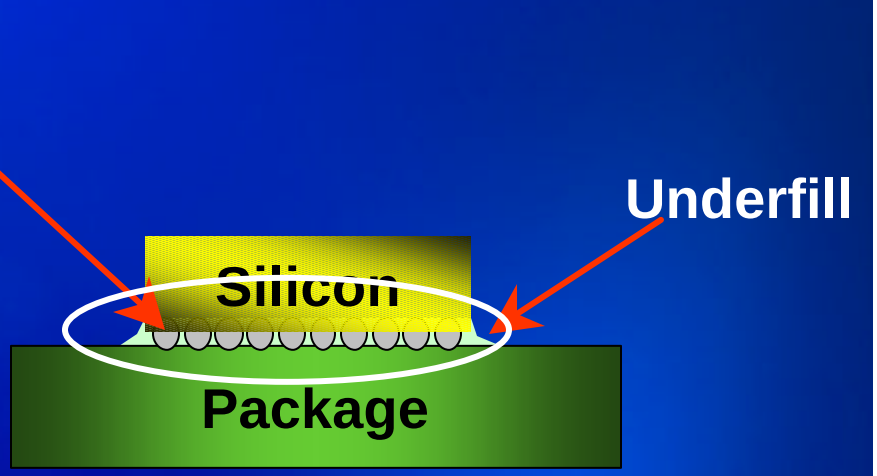
Challenge # 1

Silicon to package interconnect

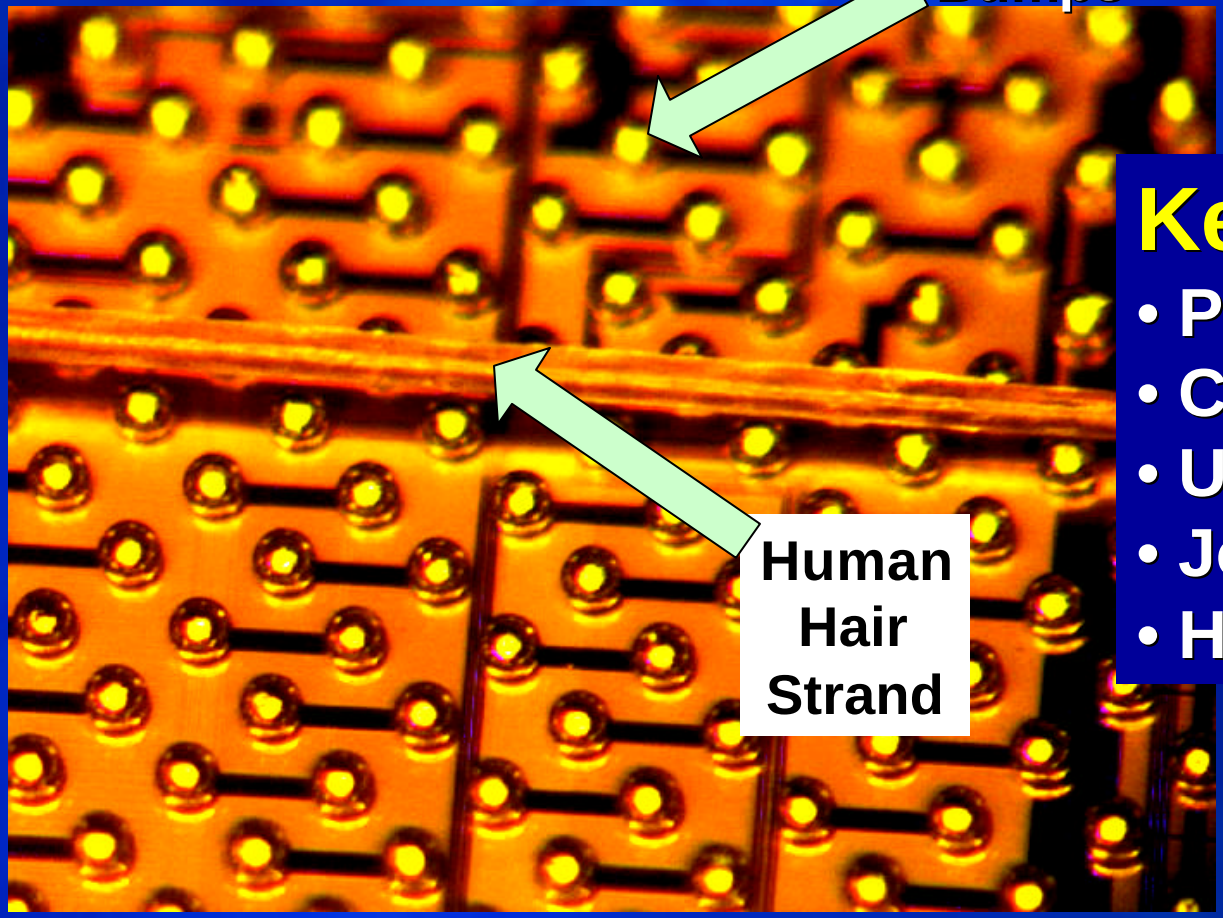
Approaching 10K flip chip bumps on a die





Driver – increased silicon functionality

Solution : Aggressive Bump Pitch Scaling to keep down die size



Key Challenges :

- Plating bumps
- Chip Attach Process
- Underfill
- Joint integrity
- HVM scalable process

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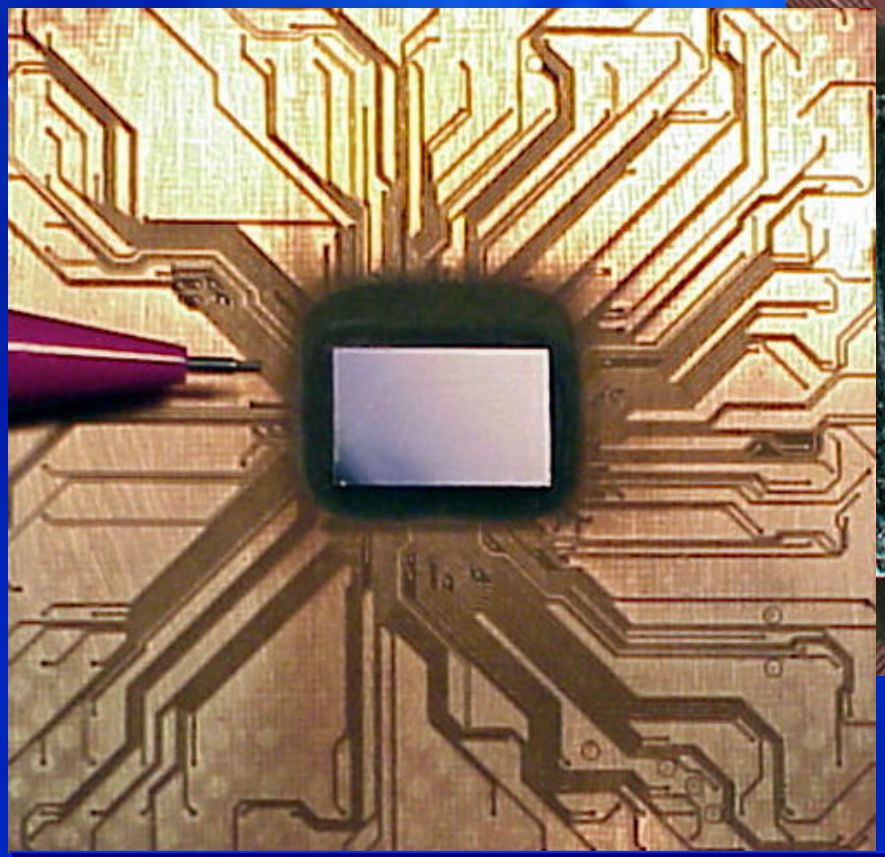
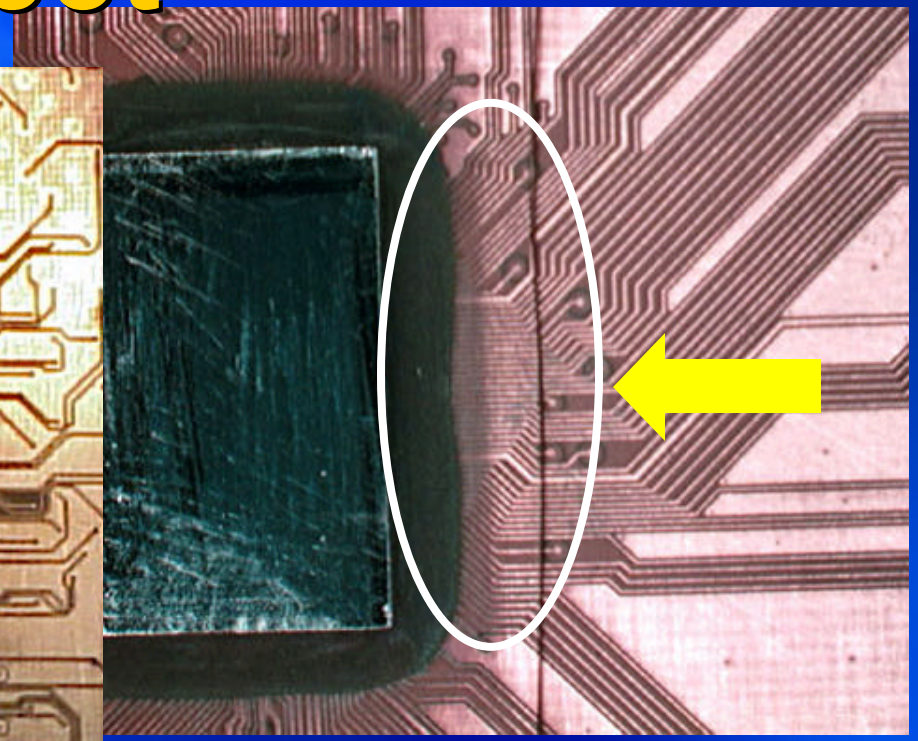
Which leads us to …

Challenge # 2

Within package Interconnect

Solution : High Density Interconnect



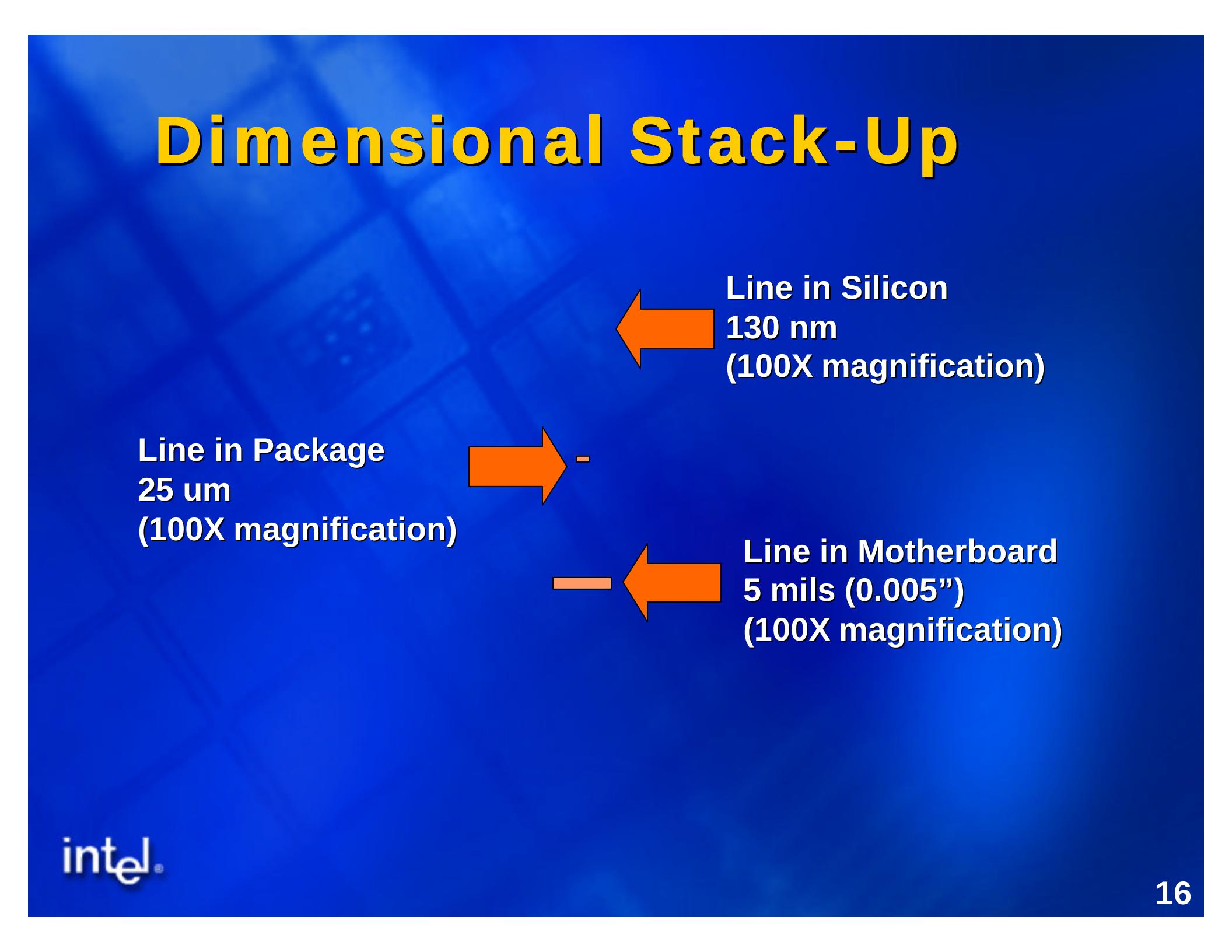


Very high escape routing density from the die

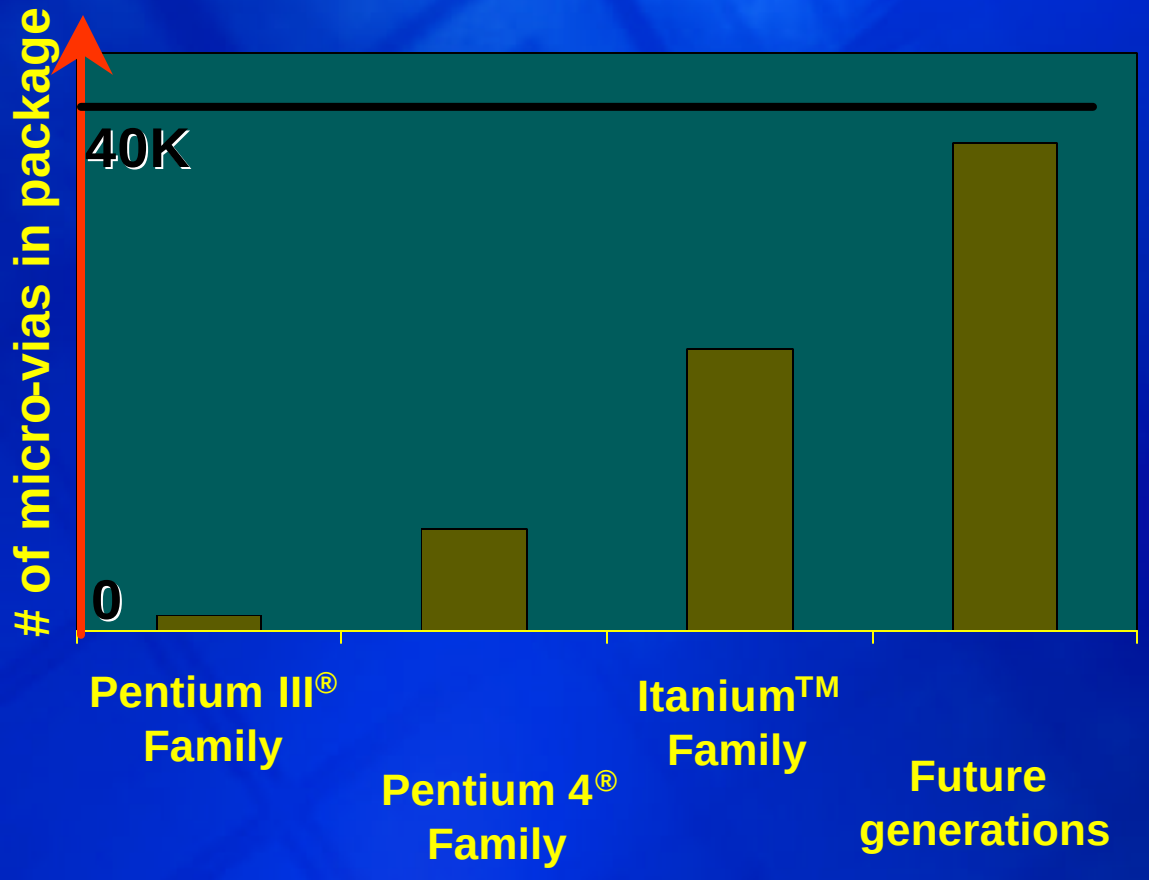
Package Traces

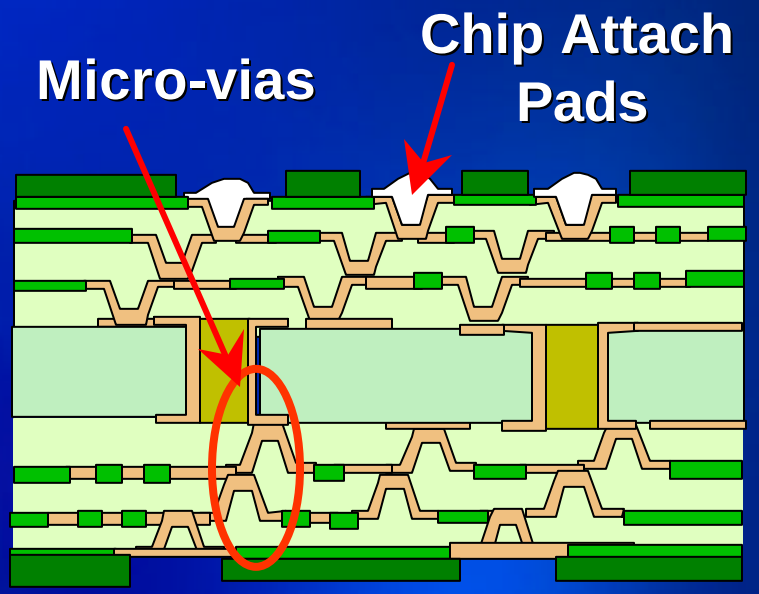
Driver : Need high wiring density

Dimensional Stack-Up



Approaching 40K micro vias inside a package

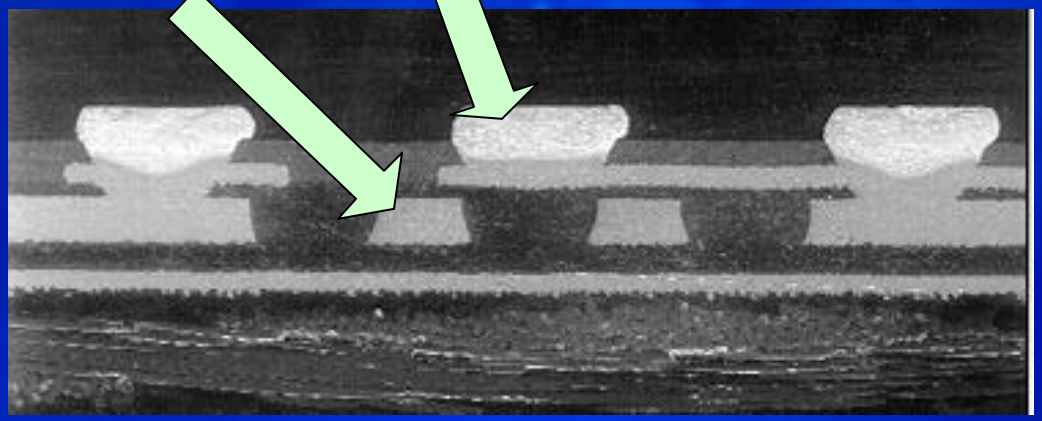




Package X-section

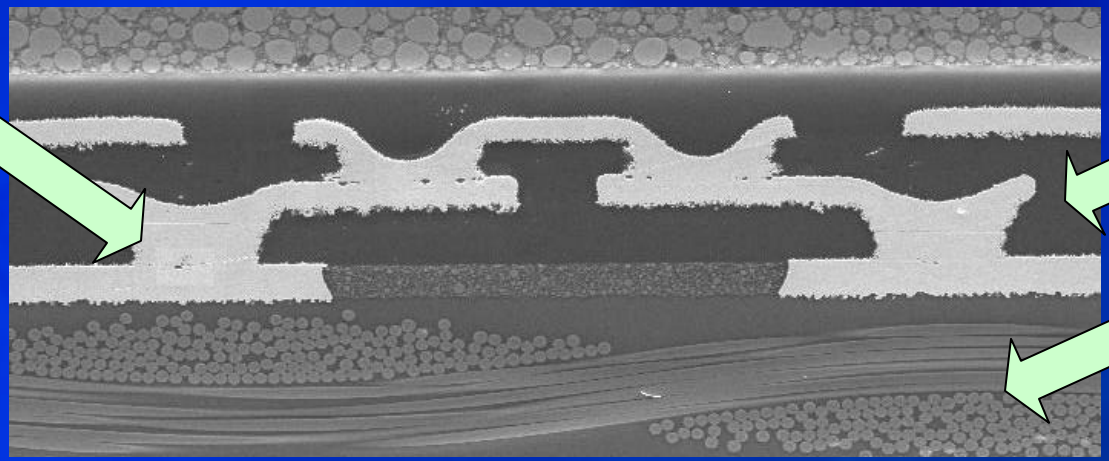
Driver – High I/O count & power supply

Solution : Advanced lithography (new term in packaging !)

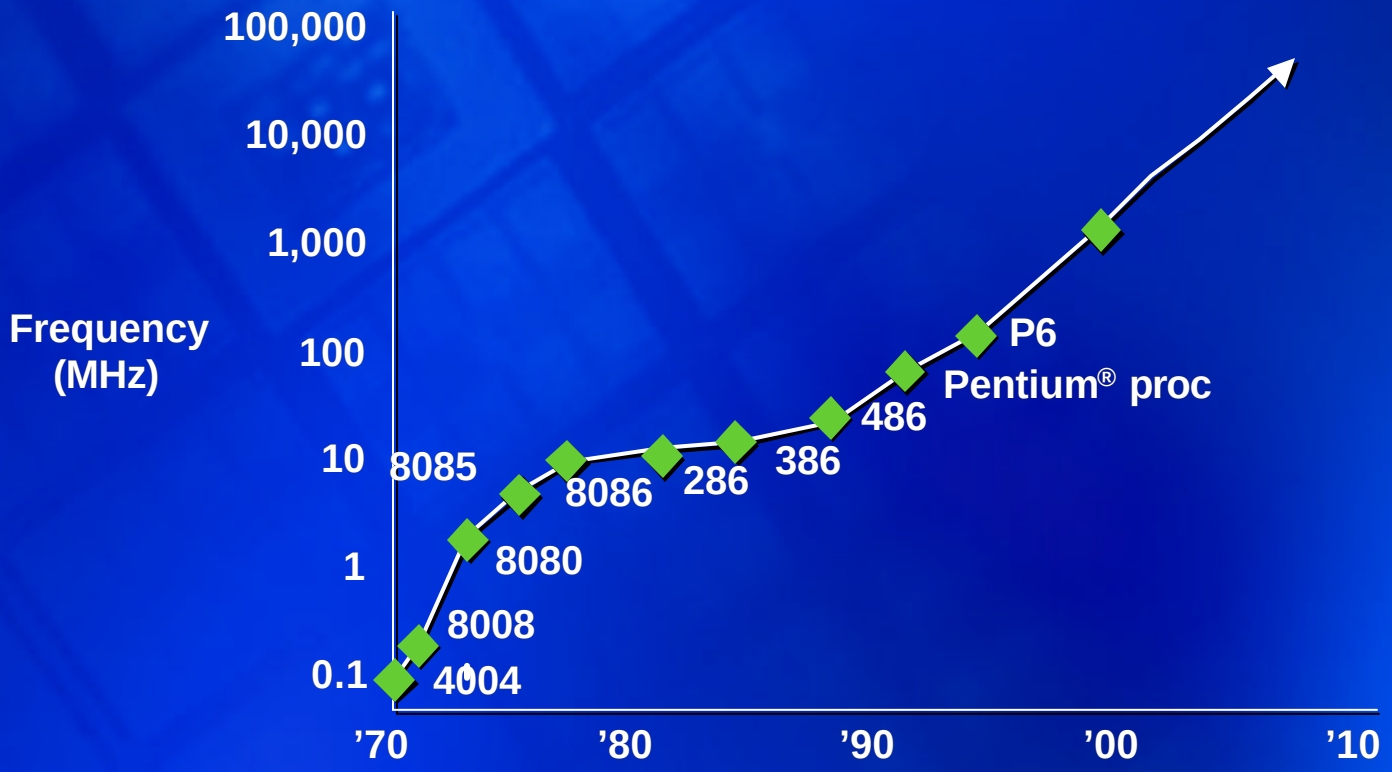


Key Challenges :

- Developing HDI (high density interconnect) at LOW COST
- High Volume Manufacturing Capable



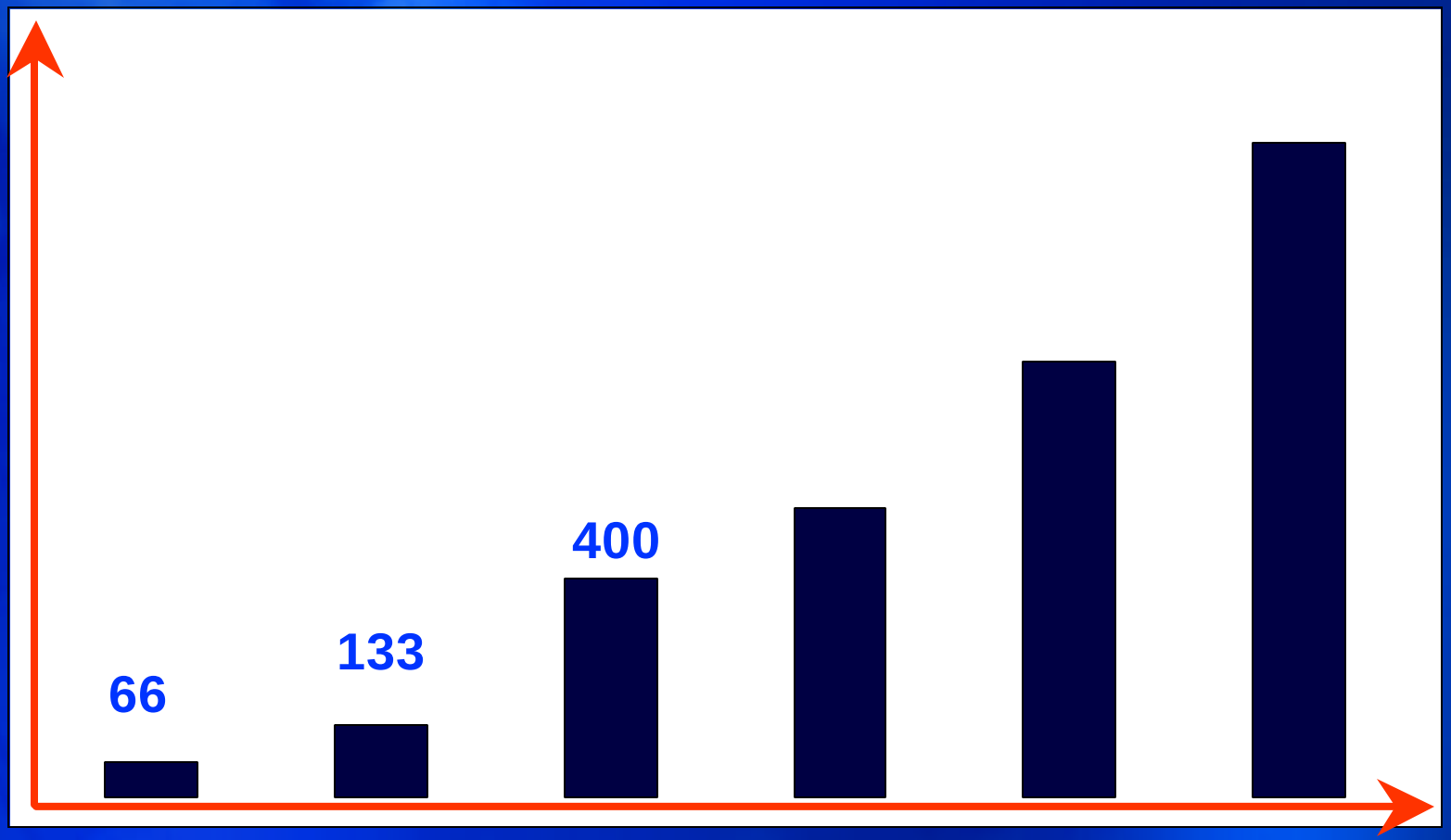
Core frequency trend ... doubling every 2 years



Source : Intel Architecture Labs

In addition ...

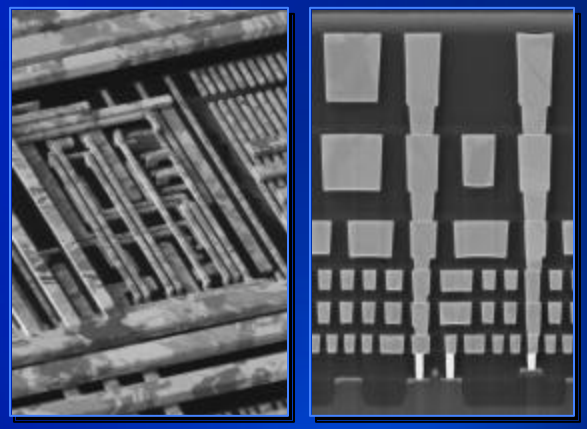
FSB frequency ramp continues



Solution : High Performance Interconnect Technology

Benefits of organic

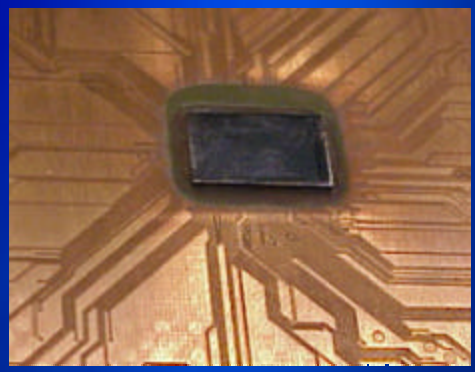
1. Copper – Low resistance
2. Low dielectric constant
3. Cheaper



High Performance Silicon Copper Interconnects

Key Challenge :

- Optimize the entire substrate architecture (material properties, layer stack-up, via placement, power bussing etc.)



Organic Packaging

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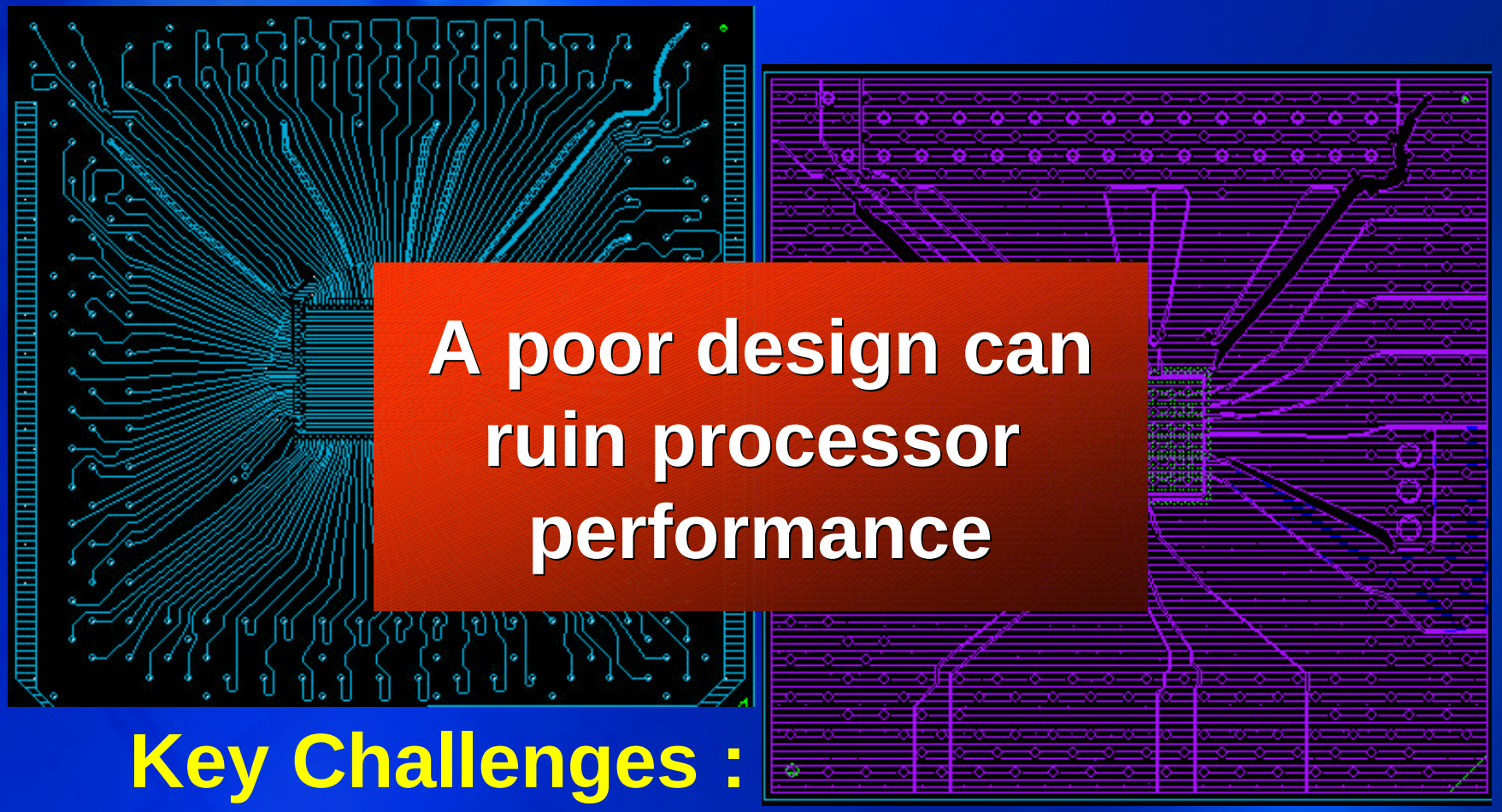
Solution : Better designs



A poor design can ruin processor performance

Key Challenges :

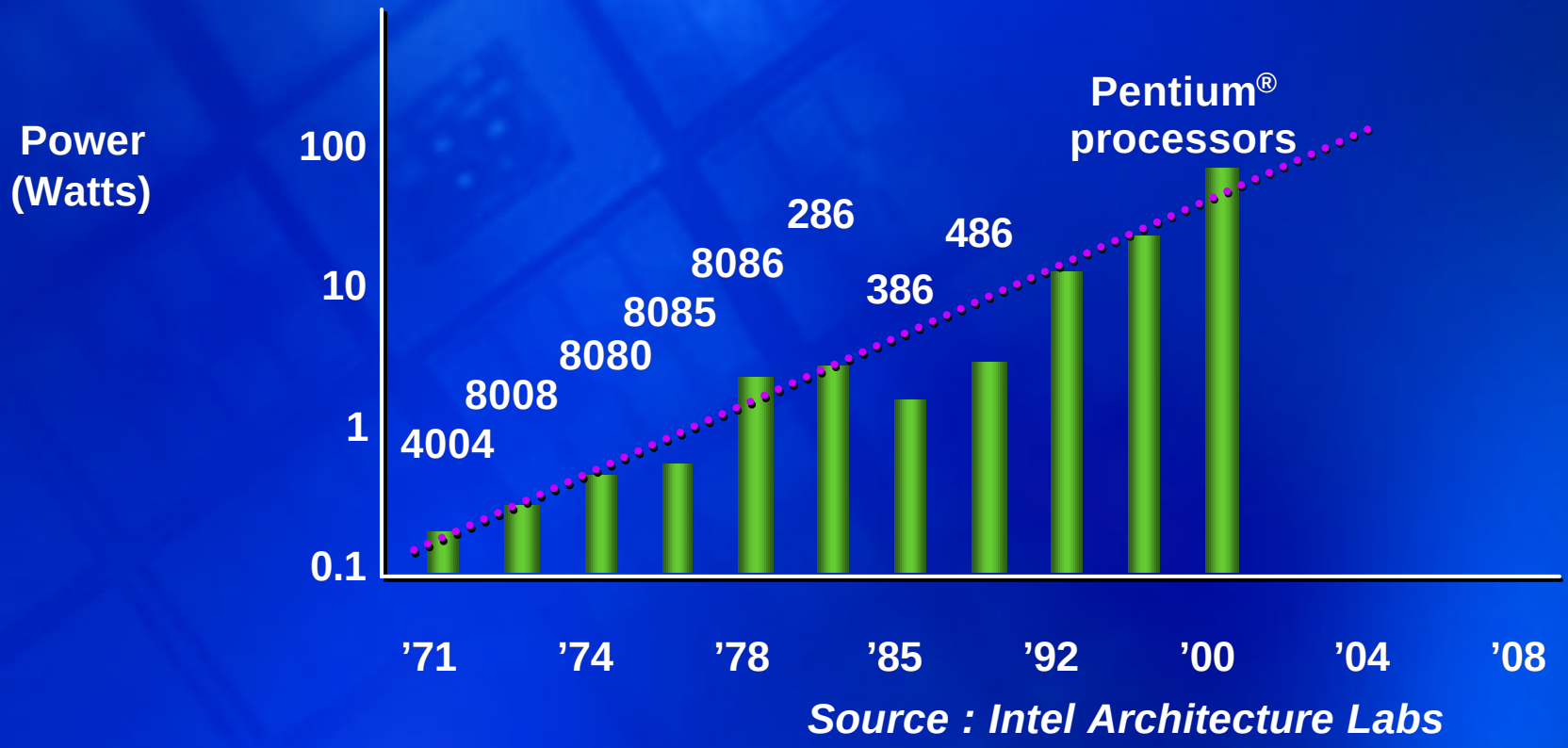
- Signal Timing
- Innovative routing – layout
- Optimizing power / ground distribution
- Co-design of the complete silicon ✍ package interconnect

Switching gears from interconnect to …

Challenge # 3

Power Management

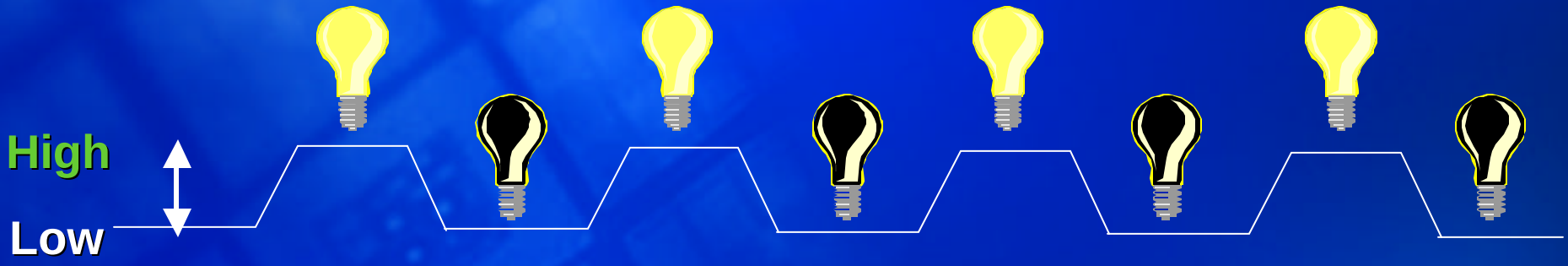
Power Increasing, silicon getting smaller



Source : Intel Architecture Labs

Two Challenges …
Getting power in & getting heat out

Importance of a quiet Power Supply



Ideal state

Reality – noise

This is what Voltage Scaling can do

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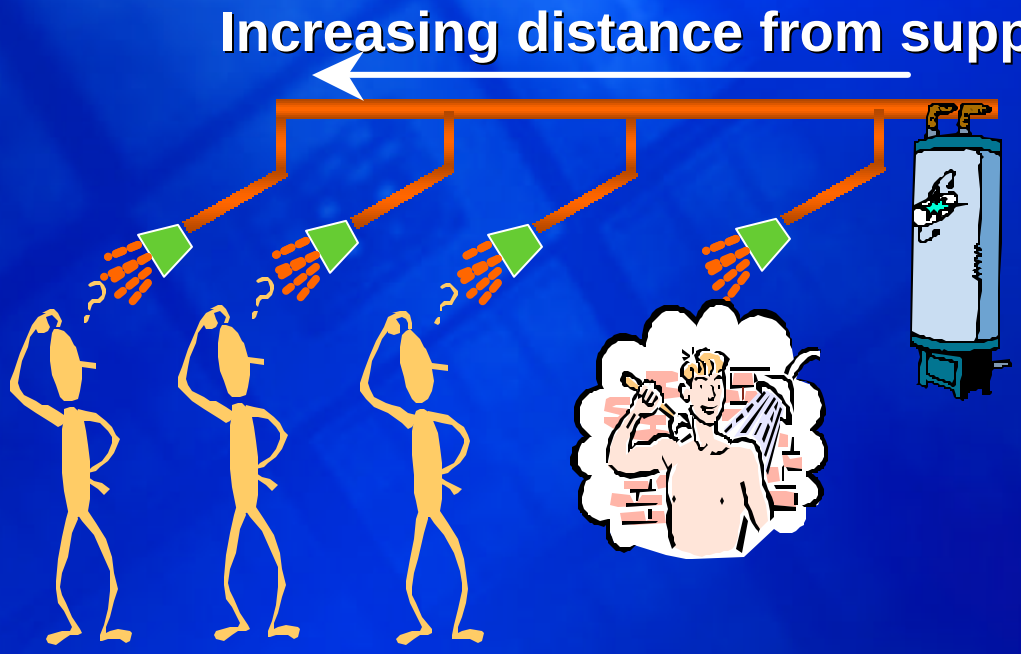
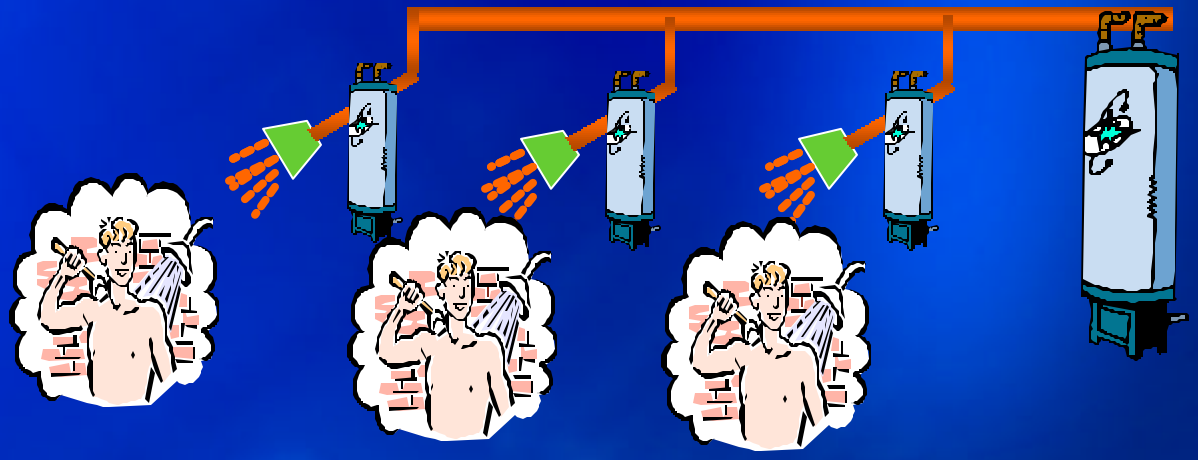
Need lots of charge, very quickly ...



Inefficient design



Close Proximity to supply

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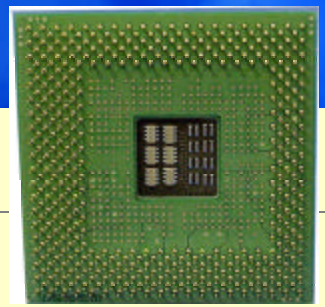
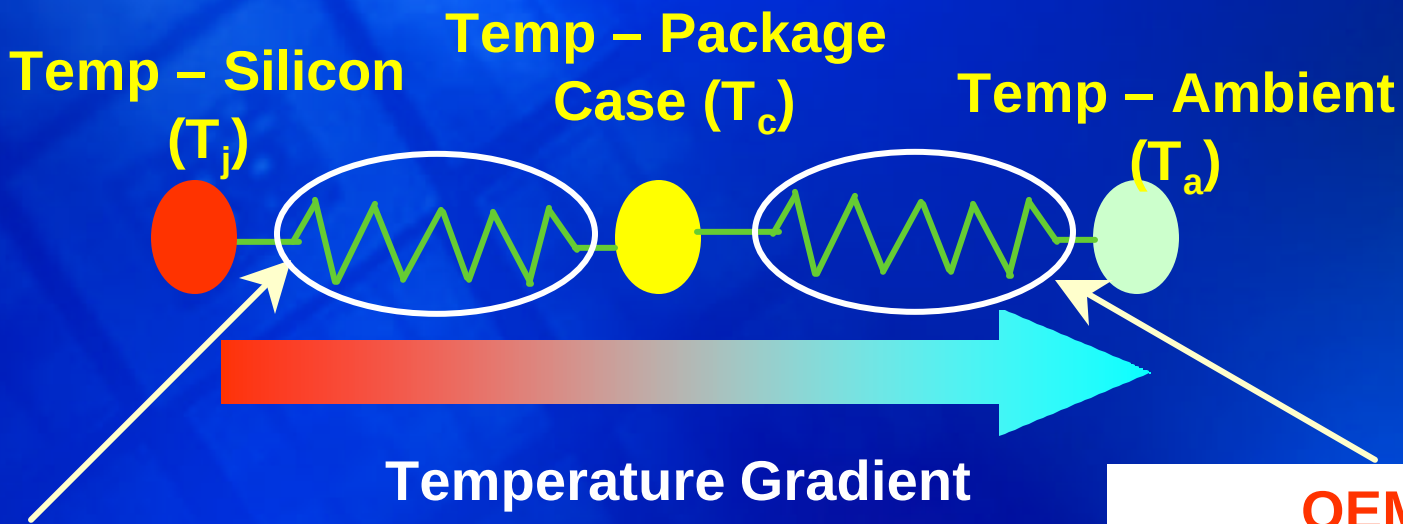
Solution : Optimize design for power delivery



Key Challenge:

- 2X improvement in capacitance and inductance needed / generation
- Need to optimize the complete silicon package integrated power delivery solution

Solution : Reduce system design burden – heat removal

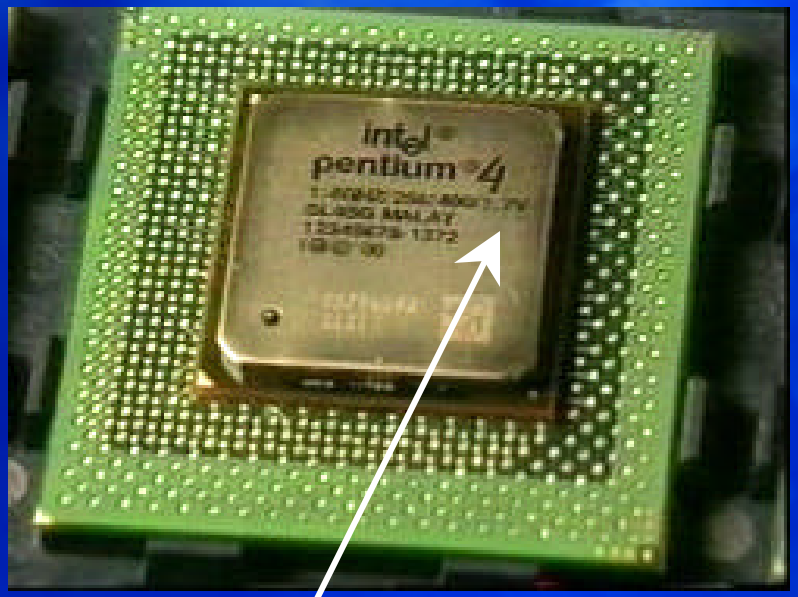


Packaging
Provide Solutions for this interface of the budget

OEM
Provide Solutions for this interface of the budget

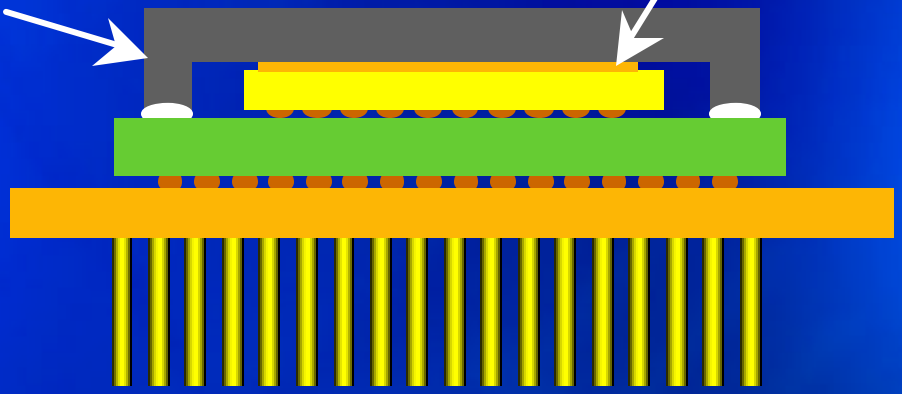
Integrated Thermal Solutions in the package reduce heat flux – easier to cool in the system

Example : Pentium4®

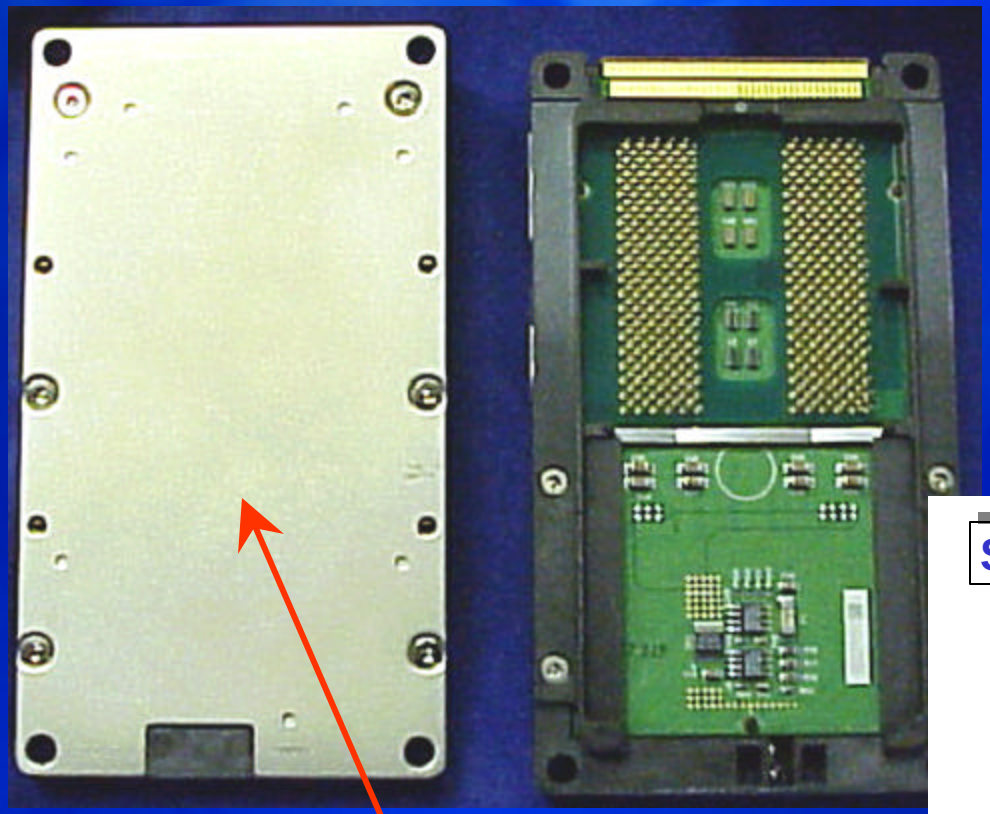


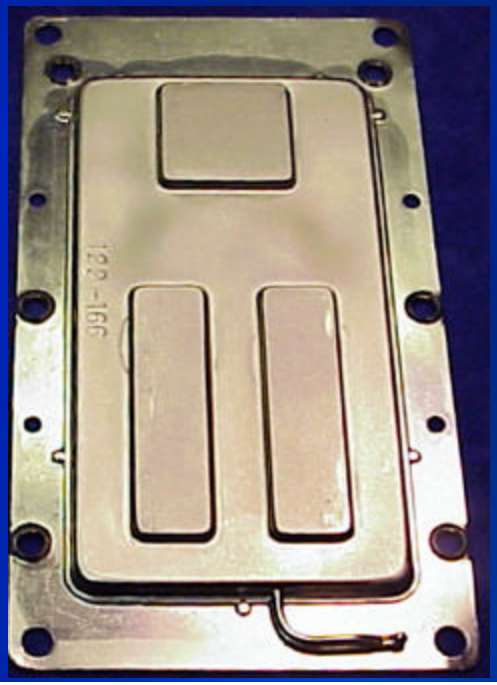
Integrated High Conductivity Heat Spreader

High conductivity Thermal Interface Material



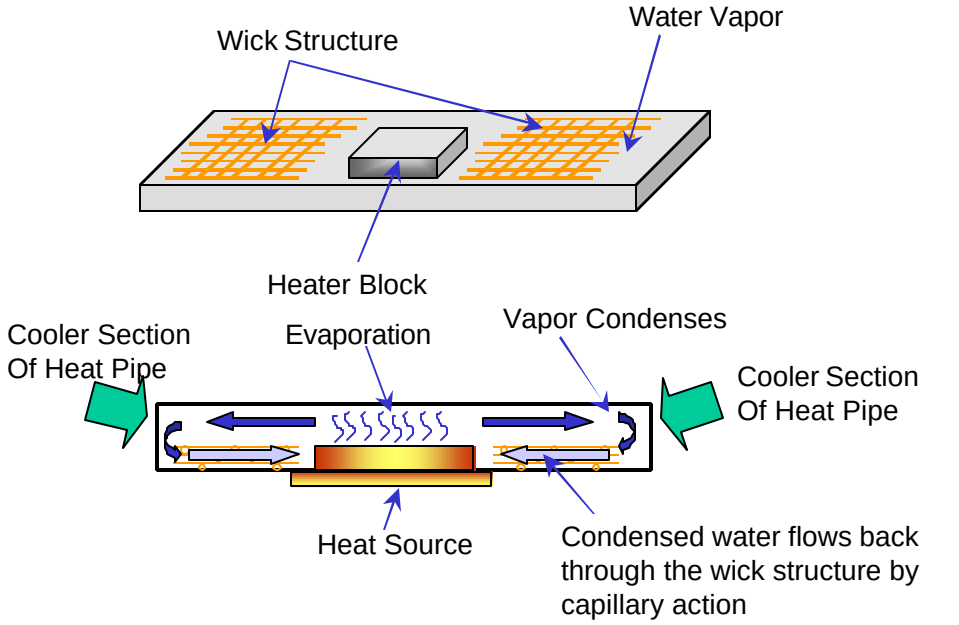
Example : Itanium®





Integrated heat pipe technology interfacing directly to the silicon

Schematic of how a typical heat pipe works



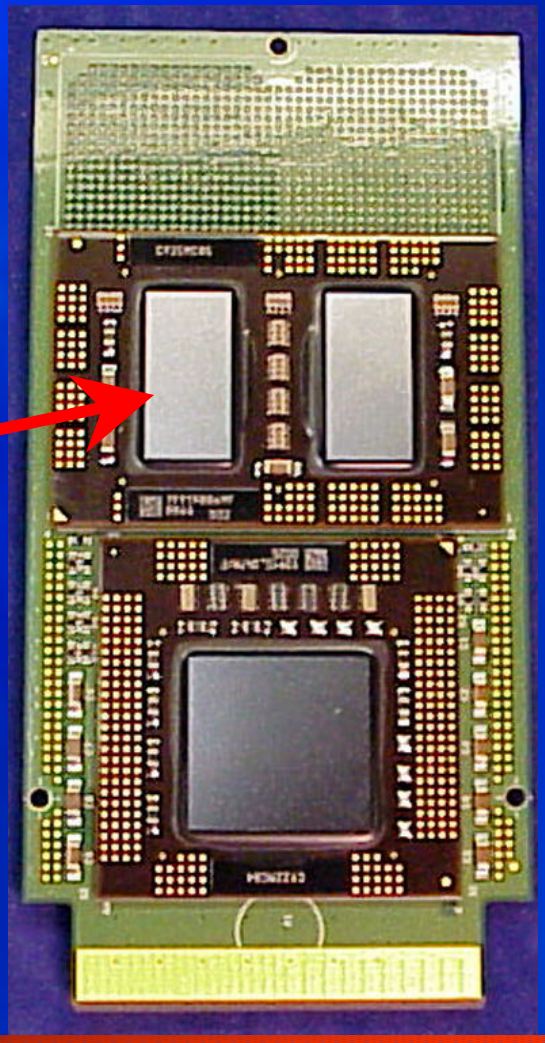
And finally …

Challenge # 4

Adding more functionality

Solution : High Density interconnect = more integration

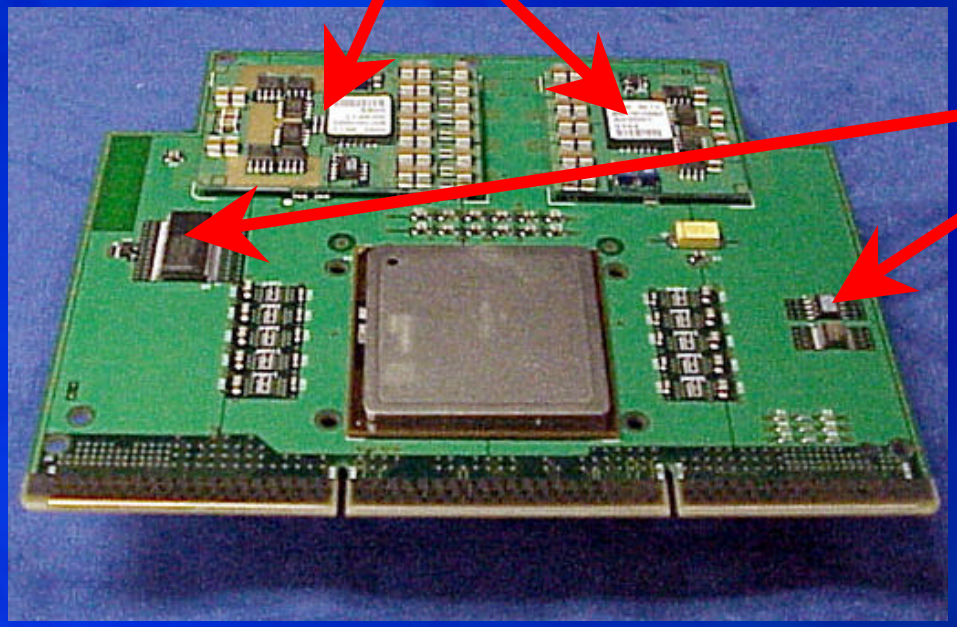
High Density Interconnect enables a large cache memory integration in a small space



Leveraging packaging instead of adding onto silicon

Solution : Massive integration = more features

On CPU Voltage regulation



RASM

In Summary ...

We talked about future Complexity and Challenges to support Moore's Law

1. Silicon to package interconnect
2. Within package interconnect
3. Power management
4. Adding more functionality

Intel's Packaging Strategy

Innovative Technology

Making Technology Affordable

Smart designs

Integrated silicon + packaging solutions

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For more information, please visit ….

Silicon Showcase
Breaking Barriers to Moore's Law

http://www.intel.com/research/silicon/packaging.htm

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