1. A scheduler has three queues; A, B and C. Outgoing link speed is 3 bits/sec
   
a. (Assume queue A wants to transmit at 1 bit/sec, and queue B at 2 bits/sec and queue C at 3 bits/sec. What actual rate are connections operating on if max-min fairness allocation is in effect?

b. You are given queue weights (A,B,C) = (1,2,3) for a set of packets P1-3 whose size is shown in bits for each queue. All packets are ready for transmission at time 0. Answer the following:
   
i. What is the order of first 5 packet transmission assuming WFQ?
   ii. How long does the transmission take?

![Packet sizes and WFQ diagram]

2. Two processors (P1,P2) are used to execute three tasks (A,B,C) with restriction that tasks A and C can execute only on P1, while B only on P2. Computation is complete when final result of computation of task C is stored in memory. Note that memory transfer time does not include the network time. You may assume that data for tasks A and B is available in on-chip cache and thus does not need to be loaded from memory at start of execution.

![Processor diagram]
a. Derive a schedule that gives the fastest time to completion of the three processes given the data flow graph.

b. What is the minimum power consumption you can obtain while still meeting the fastest completion time computed in part a? How much power savings is that over the original schedule? Assume processors can run only at two speeds – maximum and half the maximum.

4. Show why Lamport’s scalar clock is not strongly consistent the example below. Label all events with their logical clock values. Show how it can be extended to become strongly consistent on the same example. Again, make sure to label all events.

5. Schedule the following independent tasks on the single processor; the task period equals the deadline:
   T1 (start time = 2, exec time=5, period=8), T2 (0,1,10), T3 (6,1,5) using:
   a. EDF
   b. RM
   c. Determine the maximum possible execution time and period of an additional task T4(0,e,p) and show the schedule of all four tasks using:
      i. RM
      ii. EDF

6. Draw a block diagram of a CPU, memory and peripheral connected with a system bus, in which peripheral gets serviced using vectored interrupts. Assume servicing moves data from the peripheral to the memory. Show all relevant control and data lines of the bus, label component inputs/outputs clearly. Use
symbolic values for addresses. Provide a timing diagram illustrating what happens over the system bus during the interrupt.

7. You are given five tasks (T1-5) and four different HW implementations: HW1-3 (costs 25,20,30) and a processor P (cost 15). The table below shows the execution times for running each task at each HW/P unit. The task graph deadline is 90 units. Show a) fastest and b) minimum cost partitioning of tasks among HW elements and the processor. Is there an optimal solution that is faster than all others while being minimum cost? Show.

<table>
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<th>T</th>
<th>H1</th>
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</thead>
<tbody>
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<td>1</td>
<td>10</td>
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<td>20</td>
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<tr>
<td>2</td>
<td>5</td>
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<td>50</td>
<td></td>
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<tr>
<td>3</td>
<td>15</td>
<td>10</td>
<td>15</td>
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<td>4</td>
<td>10</td>
<td>10</td>
<td>15</td>
<td></td>
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<td>50</td>
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8. Your job is to design a new small (and cheap!) automated insulin regulator capable of the following major tasks:
   1. Sample blood sugar levels at regular intervals preset by the doctor (not the patient!)
   2. If levels are high, inject appropriate amount of insulin; the amount is calculated as follows;
   3. If levels are too low, inject sugar into the patient, the amount is calculated as follows:
   4. Sample sugar levels at short intervals after injection – 30s, 1min, 5min, and every 5min until 30min passes. Sound an alarm if within 30min period sugar levels don’t stabilize.
   5. Sound an alarm when either insulin or sugar containers are close to empty (10% level).
   6. Sounding an alarm includes sending a notification to the patient’s cell phone via Bluetooth, and dialing the doctor’s phone.
   7. If the patient’s sugar levels are below 50 at 30min mark, sound an alarm and dial 911.

Outline how you would perform the design process. Specifically:
   1. Draw a block diagram of HW components you’d need to use, explain why you selected the given configuration and how communication between components should be implemented
   2. Discuss what SW you would need to implement and what kind of OS, if any, might you use?
3. Is there a need for computation/communication scheduling? If so, what schedulers are appropriate?
4. What model of computation would you use for each part of the design? Illustrate.
6. Is there a need for open and/or closed loop control in the design, and if so, describe where and how it would be implemented.