CSE140 L

Instructor: Thomas Y. P. Lee
January 11, 2006

CSE140L Course Info

- Lectures
  - Wednesday 10:00-11:20AM, HSS1330
- Lab 1 Assignment Begins
  - TA's JinHua Liu (jhiu@cs.ucsd.edu)
  - Contact TAs if you're still looking for a lab partner.
  - Lab group list is maintained on the webboard.
  - TA office hour will be posted on the class webpage.
- Office Hours
  - E-mail: yunparm_lee@yahoo.com (may change later)
  - Office Hours: appointment only
- Lab Hours Start from next week
  - When: check website for detail schedule
  - Where: B230, B240, B250, B260, B270
  - You may work on your own PC. VHDL or Verilog both accepted.
- Course Policy
  - Honesty is strictly enforced. You may only discuss project with your lab partner.
Acknowledgements

- **Materials in the lecture are courtesy of the following school and people**
  - Professor C.K. Cheng of UCSD
  - Prof. Anantha Chandrakasan and Prof. Donald E. Troxel of MIT
  - *Introduction to Digital Logic Design*

CSE140L Course Info (Cont)

- **Course Text**
  - Class Website
  - Webboard, check frequently

- **Grading**
  - 70% of four labs
  - 30% of Final Exam
Agenda

● NMOS, PMOS, CMOS Inverter, CMOS NAND Gate
● Boolean Logic
● Design Styles
  ◆ ASIC v.s FPGA
  ◆ FPGA Device Structure
  ◆ IC Design Flow
  ◆ FPGA Design Flow

CSE140L Topics

● NMOS Transistor, PMOS Transistor, CMOS Inverter, CMOS NAND
● FPGA Structure
● Propagation Delay, Power Consumption, Timing Analysis
● Lab1: Combinational Circuit, Arithmetic Circuit:
  ▪ Adder, Subtractor, multiplexer, comparator
● Lab 2:Sequential Circuit:
  ▪ Counters, Flip flops, Latches
● Lab 3:Finite State Machine: Mealy Machine, Moore Machine
● Lab 4:Simple Computer System
N-Channel MOS (NMOS) Transistor

- The voltage on the gate controls the current that flows between the source and drain.
  - For NMOS, normally $V_{GS} \geq 0$
  - Voltage controlled resistance, increase $V_{GS}$, then decrease $R_{ds}$
- If $V_{GS} = 0$, then $R_{ds}$ is very high > 106 ohms or more
- N-Switch, Gate is 1, then drain D, source S are connected, Gate is 0, then drain D, source S are not connected

P-Channel MOS (PMOS) Transistor

- Same as NMOS, but source is at higher voltage than drain
  - For PMOS, normally $V_{GS} \leq 0$
  - Voltage controlled resistance, decrease $V_{GS}$, then decrease $R_{ds}$
- P-Switch, Gate is 0, then drain D, source S are connected, Gate is 1, then drain D, source S are not connected
CMOS Inverter Circuit

<table>
<thead>
<tr>
<th>$V_{in}$</th>
<th>PMOS</th>
<th>NMOS</th>
<th>$V_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0 (L)</td>
<td>CLOSED</td>
<td>OPEN</td>
<td>5.0 (H)</td>
</tr>
<tr>
<td>5.0 (H)</td>
<td>OPEN</td>
<td>CLOSED</td>
<td>0.0 (L)</td>
</tr>
</tbody>
</table>

$V_{DD} = +5.0 \, V$

PMOS

CMOS NAND Gate

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
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<td>H</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
</tbody>
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DeMorgan’s Law

- \(\neg(x \land y) = \neg x \lor \neg y\)
- \(\neg(x \lor y) = \neg x \land \neg y\)

Proof by perfect induction:

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<thead>
<tr>
<th></th>
<th></th>
<th>(\neg(x \land y))</th>
<th>(\neg x \lor \neg y)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
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An Example from Logic Diagram to Boolean Equation
ASIC v.s FPGA

- **ASIC – Application Specific Integrated Circuits**
  - Full-Custom ASICs
  - Standard Cell-Based ASICs, standard cell library based
  - Most EDA tools target for ASIC

- **FPGA - Field Programmable Gate Array**
  - General purpose logic device which can be programmed to perform to meet specific design specification

Comparison of ASIC vs. FPGA

- FPGA-macrocells consist of programmable array logic followed by a flip-flop or latch
  - Static RAM Based FPGA
  - PROM/Flash Based FPGA
  - Fused/Anti Fused Base FPGA

- Comparison

<table>
<thead>
<tr>
<th></th>
<th>ASIC</th>
<th>FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Performance</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>Turn Around Time</td>
<td>Low</td>
<td>Fast</td>
</tr>
<tr>
<td>Manufacturing Cost</td>
<td>Economical for Mass Production</td>
<td>Cost effective for low volume production. Experimental prototype</td>
</tr>
</tbody>
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FPGA Device Structure

- FPGA consist of
  - Basic Logic Cells (consists of combinational logic and I/O registers)
    - Xilinx: Configurable Logic Block (CLB)
    - Altera: Logic Array Block (LAB)
  - I/O Cells
  - Reconfigurable interconnect wires

Introduction to IC Design Flow

- According to design needs of different ICs, to choose the appropriate design flows.

<table>
<thead>
<tr>
<th>Different Semiconductor/IC Types</th>
<th>Density and Speed of IC</th>
<th>Circuits</th>
<th>HDL</th>
<th>Routing Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full Custom Design Flow</td>
<td>High Density, high speed, high sensitivity IC</td>
<td>Transistor level</td>
<td>N.A</td>
<td>Manually Routing, cost very high</td>
</tr>
<tr>
<td>Cell Based Design Flow</td>
<td>High complexity, high density IC</td>
<td>Cell Based design and library</td>
<td>HDL</td>
<td>Automatic Routing</td>
</tr>
<tr>
<td>FPGA Design Flow</td>
<td>High density IC</td>
<td>CLB or LAB</td>
<td>HDL, reconfigurable rapid prototype</td>
<td>Automatic Routing, No Mask Required</td>
</tr>
<tr>
<td>MMIC Design Flow</td>
<td>High frequency, high power IC</td>
<td>Cell based design and library</td>
<td>Cell Based</td>
<td>Manually Routing</td>
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