Discussion Session 9

CSE 141

Material in the lecture:
Copyright Henessey and Patterson

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### Questions

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### Review – Some topics covered

- ISA Decisions:
  - Instruction decoding
  - Instruction format (R, I, J, opcodes, etc.)
  - Addressing modes
  - RISC vs. CISC
- ISA’s: Stack, Acc, Reg-Reg, Load-Store

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<th>2-way 8 byte blocks, 64byte cache</th>
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Review – Performance

Major topic
Compute: IC, CPI, ET, Speedup
Amdehl’s Law
Compare Single/Multi/Pipeline
Data hazard penalty, control hazard penalty, memory CPI

Review – Single vs. Multi cycle

New instructions – implement them
Data/inst split vs. combined
RTL
FSM
Role of extra registers in multi-cycle
Microcoding
Exceptions
Modify the stages
Review – Pipelining

Why?
Role of latches
Data dependencies/hazards/forwarding
Control dependenceis/hazards
Branch Delay Slot
Static vs. Dynamic branch prediction
Exceptions
Non-MIPS pipelines

Review: Single/Multi vs. Pipelined

- Single cycle
  - CPI =
  - CT =
- Multi-Cycle
  - CPI =
  - CT =
- Pipelined
  - CPI =
  - CT =
Review – Cache

Importance of memory hierarchy
Temporal vs. Spatial Locality
Direct Mapped vs. Fully associative
Hit/Miss rates
Cache Size, Set assoc, block size, byte offset
Tag, LRU, valid, dirty bits
Different ways of handling stores

Review – Other topics

Virtual Memory – paging, TLB
Guest Lectures
Learning discussions

Questions??????