Discussion Session 7
CSE 141

Material in the lecture:
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Review

- Pipelining
- Data dependencies/Data hazards
  - There is a difference!
- Data forwarding
- Control (branch) hazards
- Static and dynamic branch prediction
- Caches

Data forwarding Review

```
add r3, r4, r2
sub r5, r3, r1
lw r6, 200(r3)
add r7, r3, r6
```

...
6.34
Split Memory access into 2 cycles from
IF  ID  EX  M  WB
200 100  50 200  50
to?

6.34 cont. 25% of branches mispredict.
What is the CPI for branches?

6.34 cont. Jumps pay 1 clock cycle of delay.
What is CPI for jumps?

6.34 cont. Loads: .5 of the next instruction
are dependent, .25 of the second next,
.125 of the third next. What is the Load
CPI?
6.34 cont. Given .25 loads, .10 stores, .11 branches, .02 jumps, .52 ALU what is the CPI for the modified pipeline?

6.34 cont. Given new CPI, what is the relative performance between single-cycle and this pipeline?

Given a 2 bit BHT, what is the prediction accuracy of branch 1. How bout a 3 bit PHT -> 2 bit BHT?
For (i=0; i<1000; i++)
If (i%2 = 10) branch1 inst;

Given a 3 bit GHR -> 2bit BHT what is (roughly) the prediction accuracy of the following code?
For (i=0; i<10; i++)
If (x>=5) blah; Branch1
If (x>=5) blah; Branch2
Branch 3
Aliasing? Two branches share same history? Share same pc? Other ideas to improve accuracy?

Questions?
Can you give sample code for which local history outperforms global?
Can you give sample code for which global history outperforms local?

For you branch prediction fans/interested in research/prospective architecture grad students, check out last years championship branch prediction competition:
http://www.jilp.org/cbp/
Given a 4 bit PHT -> 2bit BHT what is the prediction accuracy of the following code? How bout 3 bit PHT?

For (i=0; i<5; i++)
Inst1;
Branch