CSE 141L Lab 1. 8-Bit Instruction Set Architecture

Due Friday, January 24.

In this lab, you will design the instruction set for a processor. You will design the hardware for that processor in subsequent labs. This will be an 8-bit processor which you will optimize for a few simple programs (described on the next page). For this lab, you will design the instruction set and instruction formats, and code three programs to run on your instruction set. Given the extreme limit on instruction bits, the target programs and their needs should be considered carefully. The best design will come from an iterative process of designing an ISA, then coding the programs, then redesigning the ISA.

Your instruction set architecture should feature fixed-length instructions 8 bits wide. Your instruction-set specification should describe:

- what operations it supports and what their opcodes are. You should have a “halt” instruction in the ISA.
- how many instruction formats it supports and what they are (in detail -- how many bits for each field, and where they’re found in the instruction). Your instruction format description should be detailed enough that someone could write an assembler (a program that creates machine code from assembly code) for it.
- number of registers, and how many; general-purpose or specialized. The internal storage will also be 8 bits wide.
- the size of main memory.
- addressing modes supported (this applies to both memory instructions and branch instructions). That is, how are addresses constructed/calculated.

In order to fit this all in 8 bits, the memory demands of these programs will have to be small. For example, you will have to be clever to have a conventional main memory even as big as 256 bytes. However, for the programs you are going to run, you may not need all that. You should consider how much data space you will need before you finalize your instruction format. You can assume that instructions are stored in a different memory, so that your data addresses need only be big enough to hold data. You should also notice that these programs probably don’t need procedure calls and stack pointers. You should also assume that memory is byte addressable, and that loads and stores read and write exactly 8 bits.

You will write and run three programs. You can assume each starts at location 0, or you can assume that the first starts at 0, and the other two are found in memory after the end of the first program.

When implemented, this will be a single-cycle machine, so realize that there is a limit to what can be done in a single cycle. In particular, you will assume single-ported memory (a maximum of one read or one write per cycle, not both). You will also assume a register file (or whatever internal storage you support) that can only write one register per cycle. But you can, of course, read more than one register per cycle.

To simplify the ISA design process, you need only optimize for the following two goals:

1. Minimize dynamic instruction count (i.e., the number of instructions executed during the running of a particular program).
2. Simplify your processor hardware design.

You are welcome to also optimize for other things (e.g., cycle time, ease of pipelining), but if you do so, we will expect you to discuss that optimization intelligently, and these two goals should still take highest priority. You will be rewarded, in particular, for doing a good job with goal 1.

Generic ISAs (that is, ISAs that will execute other programs just as efficiently as those shown here) will be seriously frowned upon. We really want you to optimize for these programs only.

You will turn in a lab report no more than eight pages long (excluding the program listings). The report will answer the following questions. In describing your architecture, keep in mind that the person grading it has much less experience with your ISA than you do. It is your responsibility to make everything clear.
For all the labs, your report will have two parts: a lab report (in this case, your ISA description) and the answers to some questions. The format of the report is given next.

Components of lab 1:

1. Introduction. This should include the name of the architecture, overall philosophy, specific goals strived for and achieved.

2. Instruction formats. Give all formats and an example of each.

3. Operations. Give all instructions supported and their opcodes/formats.

4. Internal operands. How many registers are supported? Is there anything special about the registers?

5. Control flow (branches). What types of branches are supported? How are the target addresses calculated? What is the maximum branch distance supported?

6. What addressing modes are supported? How are addresses calculated (including instruction addresses for branches)? Give examples.

7. How large is the main memory?

8. In what ways did you optimize for dynamic instruction count?

9. In what ways did you optimize for ease of design?

10. If you optimized for anything else, what and how? (It’s OK if you didn’t)

11. Your chief competitor just announced a load-store ISA with three operands, two registers (i.e., a 1-bit register specifier), and 32 instructions (5 opcode bits). Tell me why your ISA is better.

12. What do you think will be the bottleneck in your design? That is, what don’t you have that you will miss the most if you were to have to write other, longer, programs.

13(a). What would you have done differently if you had 2 more bits for instructions?
13(b). 2 fewer bits?

14. Can you classify your machine in any of the classical ways (e.g., stack machine, accumulator, register, load-store)? If so, which? If not, give me a name for your class of machine.

15. Give an example of an “assembly language” instruction in your machine, then translate it into machine code.
for 16-18, give assembly instructions. Make sure your assembly format is either very obvious or well described, and well commented. If you also want to include machine code, the effort will not be wasted, since you will need it later. We will not correct/grade the machine code. State any assumptions you make. You cannot assume anything about the values in registers or data memory, other than those specifically given, when the program starts.

16. Assume array $V[]$, starting at address 128, consists of 63 entries, all valued between 0 and 5 (inclusive). Find the median value, and store it in location 0.
16(b). What is the dynamic instruction count of this program if there are 8 0’s, 10 1’s, 5 2’s, 15 3’s, 12 4’s, and 13 5’s?

17. Write a program that counts strings of neighboring ones in an array of 50 bytes, starting at address 64. Neighboring ones are $n$ bits next to each other which all have value one. You will count the number of strings of 2, 3, and 4 ones. For example, 00110110 has two strings of 2, and 11110110 has four strings of 2, two strings of 3, and one string of 4. Ignore neighbors across different bytes. Store the results in memory locations 2, 3, and 4, respectively.
17(b). What is the dynamic instruction count of this program? If it varies according to the number of neighbors, assume each byte contains exactly three strings of 2, two strings of 3, and one string of 4.

18. String matching. Bytes 9 and 10 contain two values. Search for those two values in order, in a 75-byte array starting at address 40. If found, store the index at which the first byte is found in address 11. If not found, store $-1$ at address 11. For example, if $M[9]$ contains 13, and $M[10]$ contains 103, and the values, starting at 40, are 1, 56, 13, 13, 0, 13, 103, … you would store 5 in $M[11]$.
18(b). What is the dynamic instruction count of this program? Assume the first value is found 3 times before the entire string is found. Assume the string is found at index 61.