You will design and implement a microprocessor!
Goals

• Practice what you will learn in CSE141
• Extend what you will learn in CSE141
  • Understand deeply how a processor works
  • See architecture play itself out in a real design
• Learn Verilog
• Get experience working on a large-scale project
• Have fun~~~
Course content

• You will implement a pipeline MIPS processor in Verilog using 5 weeks
  • It will be able to run simple but real programs compiled using gcc
  • It should be able to do simple I/O
• Make it your own processor
  • We will give you some code pieces
  • You have design the rest
  • We will give you the specifications for some others
  • You will invent, design, and implement some of your own
Course format

• Five labs
  • Due on every Thursday
• Lectures (only on Wednesdays in the future)
  • Verilog coding
  • Discussing current or upcoming labs
  • Like group office hours
• No final exam, but have a short celebration on 7/29 6p
  • Pizza
  • Prize
  • Performance
Warning!

- The course is a lot of work
  - Don’t let the 2 units fool you
- Don’t fall behind
  - The labs build on each other
  - Hard to catch if you fall behind
- Don’t wait till the last minute
  - It’s called hardware for a good reason
  - The tools are complicated, buggy in some sense...
  - Your code will be buggy, too...
Lab 1: Familiar with the tools

- Two tutorials
  - Building projects in Quartus
  - Entering and compiling Verilog
  - Simulation using ModelSim
  - Measuring the performance of your design

- Start now!
- Due: next Monday — 7/8
Lab 2: Datapath elements

• Implementing the datapath elements required for a subset of MIPS instructions
• We will give you the design and some other key components
• You will implement the design
• Due next Thursday — 7/11
Lab 3: Lights of life...

- Add control path to Lab 2
- Test your simple processor
- Execute simple programs
- Due on 7/18
Lab 4: It lives!

- Add missing pieces of MIPS
- You know how to have a working processor!
- Due 7/25
Lab 5: Let it live better!

- Pipeline your processor
- Measure the performance
- Due 8/1
Lab 6: Make it awesome!

- Optional
- Due 8/1 as well
- You can implement any other fancy features in your processor to get an A+
  - Cache
  - Dual-core
  - Branch predictor
  - Speculation
  - Dynamic scheduling
  - and etc...
Lab space and software

• We will use Altera tools for development (Quartus II)
  • Verilog editing
  • Design analysis
• We will use ModemSim for simulation
  • Simulation
  • Debugging
• Tools are huge pains
• The labs in the CSE basement have the tools installed
  • CSE B250-B270
• They are also available for free
• Lab 1 should be done independently
• Lab 2-5 should be in group of 2
  • Choose your group carefully
  • You cannot merge groups
  • Splitting up is allowed (but not encouraged)
  • Schedule an interview with TA (or Hung-Wei) before Thursday 7:30 pm every week when you’re done with the lab assignment
• We will be interviewing with the whole group
• No written report
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Instructor

• Instructor: Hung-Wei Tseng
  • Lectures: W 6p-, WLH 2111
  • Lab hours: W 6:00p-9:00p (starting next week)
    @ CSE B250-B270 or by appointment
• Check the calendar on our website
Teaching Assistant

- Ping Yin
  - Office hours: TuTh 4:30p-7:30p @ EBU3B Basement labs
  - E-mail: piyin@eng.ucsd.edu
Course resources

- Course webpage:
  http://cseweb.ucsd.edu/classes/su19/cse141L-a/
- TritonEd:
  http://tritoned.ucsd.edu
  we use tritoned to turn in reports, record grades.
- Discussion board:
  - Search before ask
  - https://piazza.com/class/jxfmqa8wajk20v