Homework #3
CSE 140 – Summer Session 2 – 2017
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Only a subset of questions will be graded

1) Design a Ripple-Carry 3-bit adder using 2 Full Adders, 2 Half Adders and an OR gate. You can draw full adders and half adders as blocks labeled with “FA” and “HA” respectively. Draw a clear diagram.

2) Design a flip flop which has two control inputs called P and N. This PN flip flop performs the following operations:

if (P,N) = (0,0), reset the output to zero;
if (P,N) = (0,1), hold the previous output;
if (P,N) = (1,0), invert the previous output;
if (P,N) = (1,1), set the output to one.

   a. Fill out a truth table for this circuit
   b. Provide the characteristic equation for the PN flip flop
   c. Show how we can implement D-FF using this PN-FF
   d. Show how we can implement PN-FF using D-FF and other gates, muxes, etc.

3) Use the types of decoders specified below with a minimal number of other gates to implement a function which gives the following output:

   ● 1, if the binary representation of any number less than 16 contains even number of 1’s
   ● 0, otherwise.

   a. Using 3:8 decoders
   b. Using 2:4 decoders
4) Consider an 4-bit comparator with outputs for “P<Q” and “P>Q”.

Design a 8-bit comparator with outputs “P>Q”, and “P<Q”, using two copies of the above 4-bit comparator, NOR gates, and INVERTERS.

5) Design a 1-bit full adder (with carry in and carry out) using two 4x1 multiplexers.

6) Analyze the behavior of a level-sensitive SR latch (which diagram is shown below) and complete the timing diagram with the correct waveforms.