CSE140L: Components and Design Techniques for Digital Systems Lab

Power Consumption in Digital Circuits

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About the final

Friday 09/02 at 11.30am in WLH2204

~2hrs exam including (but not limited to):
- True/False questions
- Multiple choice questions
- Code analysis
- Code writing

What to expect:
- Questions on the topics explained in class
- Questions on the topics of your homeworks, including the “general questions” sections
Design space of digital circuits

When designing circuits, we want to achieve a desired functionality while looking for tradeoffs between the following:
- **Performance** (e.g. timing, delay, clock frequency)
- **Power consumption**

![Power vs Performance tradeoff chart]

- **Power**:
  - Slow, power hungry
  - Slow, low power
- **Performance**:
  - Fast, power hungry
  - Fast, low power

Power and performance are closely related. In general, you cannot decrease one without increasing the other.

Your design might have a number of additional constraints:
- **Area**
- **Accuracy**
What is power?

In physics: Power is the rate of doing work (i.e. the rate of consuming Energy)

\[ P = \frac{E}{t} \]

Units of measure:
- Power: Watt
- Energy: Joule

1 Watt = 1 Joule / 1 second

Power is a function of time, energy is not!

Energy consumed in a time interval \([t_0, t_1]\):

\[ E = \int_{t_0}^{t_1} P(t)dt \]
Power consumption of circuits

- The definition of “work done per unit time” is still valid
- We need to investigate more into details what the “work done” is in electrical circuits

\[
\text{Work done} = E = V \cdot Q
\]

\[
P = \text{work done per unit time} = \frac{E}{t} = \frac{V \cdot Q}{t} = V \cdot I
\]

Example: Resistor

Conservation of energy:
energy cannot be created or destroyed, but can be altered from one form to another

Electrical energy dissipated on a resistor turns into heat
Example: CMOS inverter

There is power consumed every time there is a current flowing (I) subject to a difference of electric potential (V). Remember:
- Transistors have an intrinsic resistance
- We model the output connection of gates with a “load capacitance”

When is that the inverter is consuming electric power?
- When the output is changing its values (and transistors are switching)
- Also, when transistor are OFF, they are still “leaking” some current

Where is this power going to?
- Dissipated as heat
- Spent for “charging” the load capacitor
Power consumption

- Power dissipation in CMOS circuits comes from two components:

  - **Dynamic Power**
    - Takes place when transistors are switching
      - Charging and discharging (switching) of the load capacitance
      - “Short-Circuit” current while both pMOS and nMOS networks are partially ON

  - **Static Power**
    - Given by “leakage currents”
      - Subthreshold conduction
      - Tunneling current
      - Leakage through reverse biased diodes
Dynamic power

Dynamic power can be modeled by a relatively simple mathematical model:

\[ P_{\text{dynamic}} = A C V^2 f \]

- \(V\): Operating voltage of the circuit
- \(f\): Operating frequency (i.e. clock) of the circuit
- \(C\): Capacitance
  - Equivalent capacitance of the circuit
  - Once the circuit is built, this is a fixed property of the circuit
  - It is a function of number and dimension of wires and transistors
- \(A\): Activity factor
  - It is a term that accounts for “how much” the transistors are switching
  - It is a property of the “workload” of the circuit (for example, the application you are executing on your computer)
Static power

Static power can be expressed by the product of voltage times leakage current:

\[ P_{\text{static}} = V I_{\text{leakage}} \]

- The leakage current \( I_{\text{leakage}} \) is a rather complicated term, which is itself the sum of different contributions (depending on the physical origin of the leak).
  - Subthreshold leakage
  - Gate leakage
  - Junction leakage
  - Contention current

- Such contributions have much more complicated equations, which depend on many technological and physical parameters of transistors
Problems related to power consumption

- Data centers:
  - Electricity bill $$$

- Mobile devices:
  - Battery

- Common problem: Higher temperature
  - Temperature increases linearly with power.
  - Data centers: fans, cooling systems, AC → even higher electricity bill!
  - Mobiles: Overheating, discomfort for the user, risk of damaging the device.
  - Higher temperature → higher static power consumption!
How to reduce dynamic power consumption?

Dynamic power reduction:

- Decrease activity factor
  - Selective clock gating
  - Drawback: if the system transitions rapidly from an idle mode to a fully active mode a large $\frac{di}{dt}$ spike will occur
- Decrease switching capacitance
  - Small transistors
  - Careful floor planning to reduce interconnect
- Decrease power supply
  - Adjust voltage depending on the operating mode
- Decrease operating frequency
  - Modern OS and processors support Dynamic Voltage Frequency Scaling (DVFS)

\[ P_{\text{dynamic}} = A C V^2 f \]
Example 1: GPU, power and FPS

Your operating system can control the operating frequency and voltage of your GPU while playing 3D games. This would also impact the quality of the game, referred to as Frames per Second (FPS). For the game to be playable, the FPS should be at least 60.

Assume that FPS increases linearly with frequency: $FPS = b \times f$

Where $b = 0.5$

Assume the GPU has a range of frequency [100 300] MHz, and can switch only between fixed Voltage-frequency pairs.
Example 1: GPU, power and FPS

\[ FPS_{target} = b \times f_{target} \]

\[ f_{target} = \frac{FPS_{target}}{b} = \frac{60}{0.5} = 120\text{MHz} \]

\[ f_{selected} = 150\text{MHz} \]
\[ V_{selected} = 0.95\text{V} \]

Assuming that \( A = 0.8 \), \( C = 120\text{pF} \), and that the static power is constant and equal to 5W, calculate the total power consumption

\[ P_{dynamic} = ACV^2f = 0.8 \times 120 \times 10^{-9} \times (0.95)^2 \times 150 \times 10^6 \approx 13W \]

\[ P_{total} = P_{dynamic} + P_{static} = 13W + 5W = 18W \]
Example 2: Smartphone under the sun

If your phone is under the sun, the temperature of the processor is 70 C. When it is under the shade, the temperature is 40 C. Assume that the static power is described by:

\[ P_{static} = a e^{bT} \]

Where \( a = 1 [W] \) and \( b = \frac{1}{50} \left[ \frac{1}{C} \right] \)

Assuming that the battery has 2000J of residual capacity, how long do you increase the battery lifetime by keeping it on the shade? (assume that the dynamic power is zero and that the power consumption of other components is negligible)

\[ t (40 \, \text{C}) = \frac{E}{P_{static}(40 \, \text{C})} = \frac{2000J}{2.22W} \approx 900 \, s \]

\[ t (70 \, \text{C}) = \frac{E}{P_{static}(70 \, \text{C})} \approx 500s \]
Power consumption of digital circuits has two main components:
- Dynamic power
- Static Power

Dynamic power is expressed as $P_{dyn} = ACV^2f$

Static power is expressed as $P_{static} = VI_{leakage}$
- Static power increases exponentially with temperature
SEELAB: System Energy Efficiency Lab

Head of the Lab: Professor Tajana Simunic Rosing

Smart Cities, Smart Grids, Internet of Things

Data Centers and High Performance Computing

Mobile Devices

Check out the website: http://seelab.ucsd.edu/index.shtml