CSE140L: Components and Design Techniques for Digital Systems Lab

Final Review

Pietro Mercati
Example of True/False questions

- Everybody should submit his/her CAPE evaluation because that is an extremely important feedback for the university and for instructors to improve the quality of teaching T
Example of True/False questions

1) Verilog is a HDL T
2) The LHS of a procedural assignment should always be a reg T
3) Verilog is used to describe a behavior that is synthesized into real hardware T
4) A reg variable is a register F
5) Dynamic power consumption does not depend on operating voltage F
6) The TinyCPU lab homework was an example of combinational circuit F
7) Mixing blocking and non-blocking assignment in the same procedure is highly recommended F
8) Wire and reg are data types in Verilog T
9) $display is a keyword that automatically synthesize a display for your digital circuit F
10) Xylinx is a major FPGA vendor T
11) An FPGA is a type of HDMI adapter F
12) If “ `timescale 1s/1ms ”, then #100 is a delay of 100ms F
Examples of Multiple Choice Questions

1) A FSM with 6 states requires at least:
   a) 2-bit states
   b) 3-bit states
   c) 4-bit states
   d) None of the above

2) The value of a displayed by the following code at time 30 is

   ```
   #20 a <= 10;
   #5   a <= 20;
   ```

   a) 10
   b) 20
   c) 5
   d) None of the above
3) The value of a displayed by the following code at time 30 is

```java
#20 a = 10;
#5   a = 20;
```

a) 10
b) 20
c) 5
d) None of the above
Examples of Multiple Choice Questions

4) What’s the keyword in Verilog testbenches to indicate that interrupts the simulation with the possibility of resuming it?
   a. $finish
   b. $monitor
   c. $stop
   d. $fish
   e. None of the above

5) Compared to the carry-lookahead adder, the ripple-carry adder is:
   a. Slower
   b. Faster
   c. Smaller
   d. Bigger
   e. a & c
   f. a & d
   g. b & c
   h. b & d
Example: code analysis

Which mistakes are contained in the following code?

```
Module my_multiplier(a, out, in);
input [3:0] a;
input clk;
output in;
reg in;

always@(negedge clk) begin
    if (out == 1)
        in <= a;
    else
        in <= in+1;
end
```

1) out is missing from port declaration (it should be an input port)
2) clk should be in the port list
3) reg in should be reg [3:0] in
4) endmodule is missing
5) This design needs a reset
Example: from code to circuit

module my_circuit(a, b, in1, wire4);
input a, b, wire4;
output in1;
reg in1;
wire out3;
reg out98;

always begin
   out98 <= a & b;
   in1 <= out98 | out3;
end
assign out3 = a ^ wire4;
endmodule
Example: from state diagram to code

```verilog
module my_fsm(C, clk, reset, out);
input C, clk, reset;
output out;
reg out;
reg [1:0] state;
reg [1:0] next_state;

parameter S0 = 2'b00;
parameter S1 = 2'b01;
parameter S2 = 2'b10;

always @(posedge clk) begin
  if (reset)
    state = S0;
  else
    state = next_state;
end

always @(C or state) begin
  case(state)
    S0:
      if (in == 0)
        next_state = S0;
      else
        next_state = S1;
    S1:
      if (in == 0)
        next_state = S0;
      else
        next_state = S2;
    S2:
      if (in == 0)
        next_state = S1;
      else
        next_state = S2;
  endcase
end

always @(state)
  case(state)
    S0: out = 1;
    S1: out = 0;
    S2: out = 0;
  endcase
endmodule
```
CAPE

Please submit your CAPE evaluations!
Summary of CSE140L – SU216

• Transistors and circuit delays
• Basics of Verilog: operators, syntax
• Quartus IDE + Modelsim simulation (HW1)
• Implementation of Verilog modules (HW2)
• Implementation of testbenches (HW2,3,5)
• Re-using modules to implement larger modules (instantiation + explicit module connection) (HW3,4)
• Implementation of a large project using smaller modules as building blocks (HW4)
• Implementation of Mealy and Moore FSM (HW5)
Digital circuits can be described using HDLs and synthesized automatically using IDEs such as Quartus.

HDLs are different from programming languages.

You can (and actually should) use and re-use components that you already implemented to build larger components.
Good Luck for the Final Exam!