

Lab 5 preview

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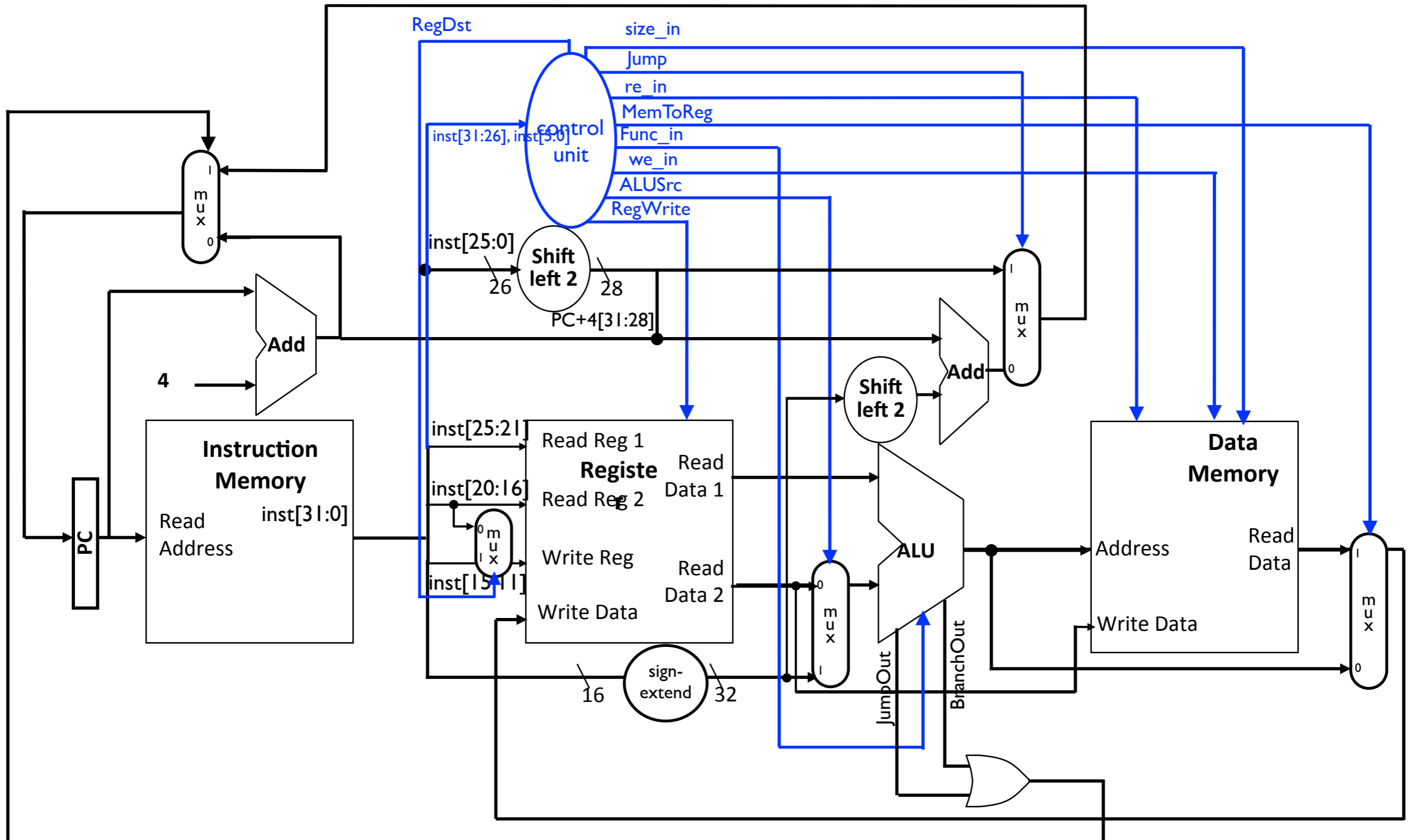
Announcement

- Lab 4 due Thursday before 7pm!
 - Interview with any of us, and send a copy of your source to the person who you interviewed with
- Lab 5 & 6 due next Thursday
 - No extension
- Come and have some pizza together next Friday @ 6p!

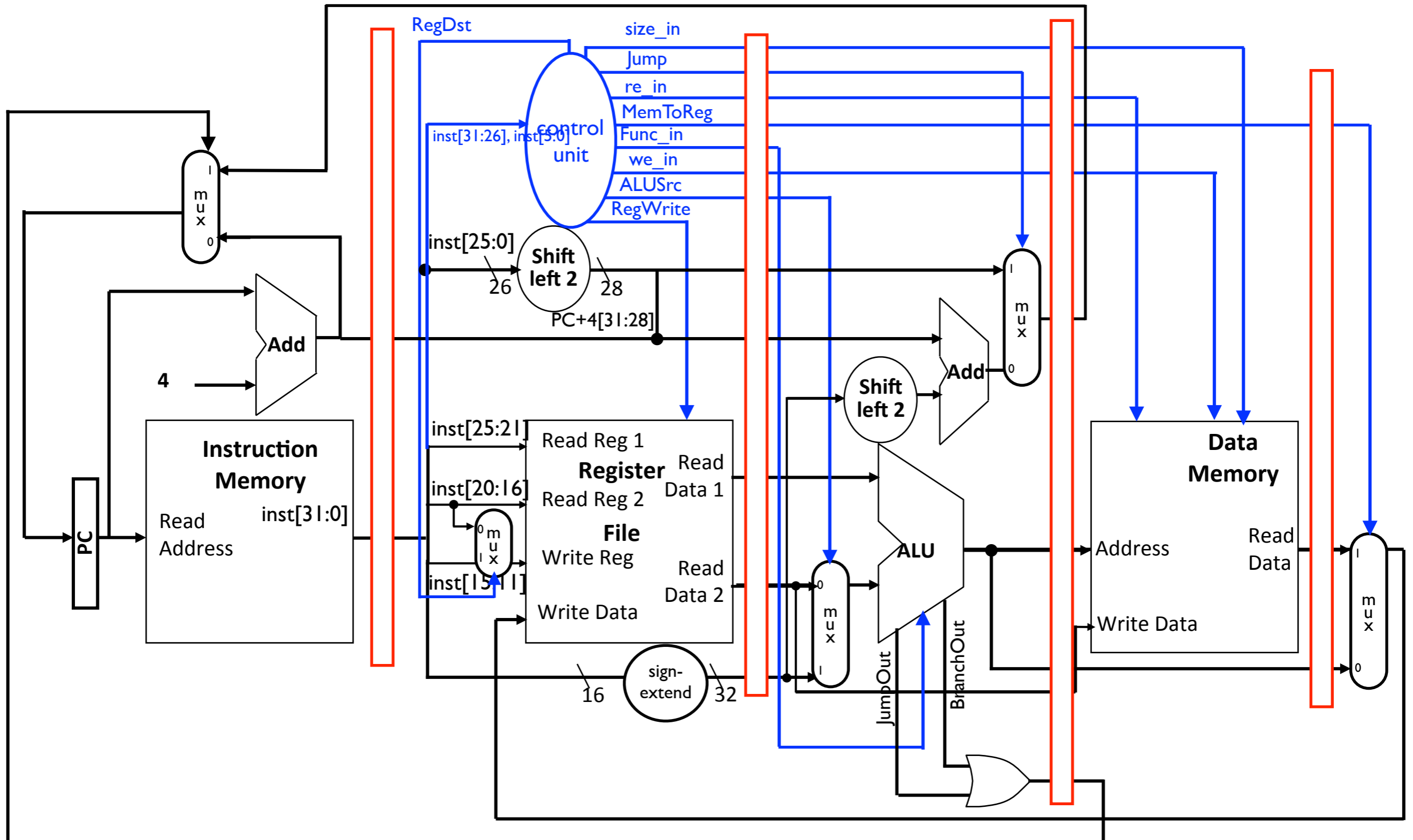
In Lab 5...

- Pipeline your processor
 - Teach it “walk”, and teach it “fly”
 - A working pipeline processor is better than a crappy 5-stage
 - Your processor does not have to be 5-stage
 - Please complete the lab as soon as possible

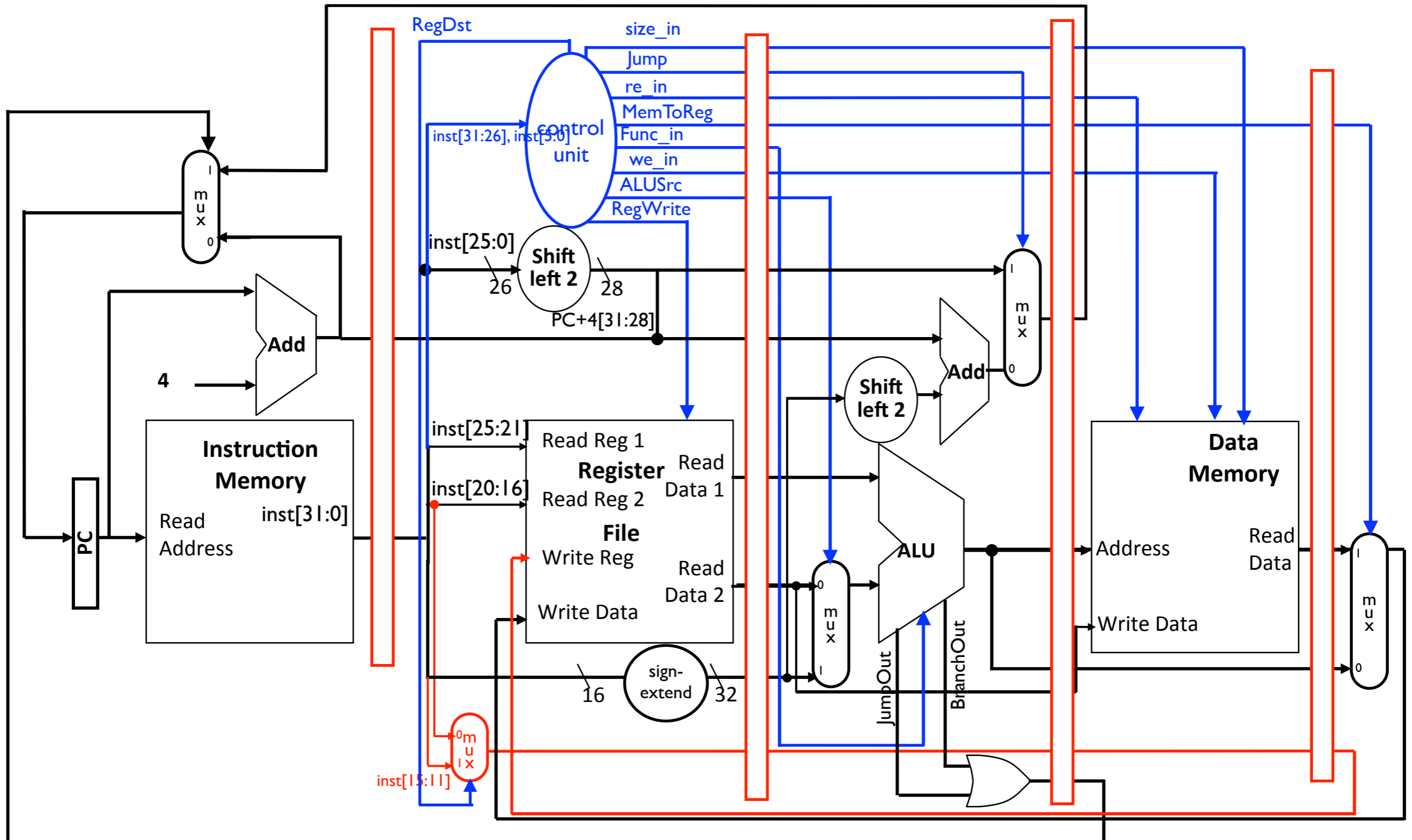
In lab4, you already have...



In lab5, we are going to pipeline it!



It's not just adding pipeline registers!



Dealing with hazards

- In standard 5-stage MIPS pipeline, you will meet
 - Data hazard
 - Stall
 - Data forwarding (bonus)
 - Control hazard
 - Stall
 - You may move branch resolution to the ID stage
 - Branch prediction (bonus)

Instead of 5-stage

- 4-stage
 - For example, IF, ID, EX+MEM, WB
 - Fewer stall conditions
 - Longer cycle time
- 3-stage
- 2-stage
 - IF+ID, the rest
- IF alone cannot be a pipeline stage

Benchmarks

- In this lab, we provide three following benchmark programs in <http://cseweb.ucsd.edu/classes/su14/cse141L-a/Media/lab5/lab5-files.zip>
 - No branch hello world
 - Hello world with branch
 - Fibonacci number
 - GCD
 - Start with PC 0x400000
- A testing script

Interview questions

- Show the schematics
- Show the waveforms of three benchmarks until the end
- Measure the IC, total cycles, CPI
- Report the Fmax
 - We can calculate the performance of your processor!

Lab 6: Optimization!

- Data forwarding
- Branch prediction
- Cache
- Superscalar
- Special bonus for fastest processor

Don't forget to come
by 9/5 6pm @ WLH
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