CSE 141 L: Building a microprocessor

Hung-Wei Tseng
You will design and implement a microprocessor!
Goals

• Practice what you will learn in CSE141
• Extend what you will learn in CSE141
  • Understand deeply how a processor works
  • See architecture play itself out in a real design
• Learn Verilog
• Get experience working on a large-scale project
• Have fun~~~
Course content

- You will implement a pipeline MIPS processor in Verilog using 5 weeks
  - It will be able to run simple but real programs compiled using gcc
  - It should be able to do simple I/O
- Make it your own processor
  - We will give you some code pieces
  - You have design the rest
  - We will give you the specifications for some others
  - You will invent, design, and implement some of your own
Course format

• Five labs
  • Due on every Thursday

• Lectures (only on Wednesdays in the future)
  • Verilog coding
  • Discussing current or upcoming labs
  • Like group office hours
Warning!

- The course is **a lot** of work
  - Don’t let the 2 units fool you
- Don’t fall behind
  - The labs build on each other
  - Hard to catch if you fall behind
- Don’t wait till the last minute
  - It’s called **hardware** for a good reason
  - The tools are complicated, buggy in some sense...
  - Your code will be buggy, too...
Lab 1: Familiar with the tools

• Two tutorials
  • Building projects in Quartus
  • Entering and compiling Verilog
  • Simulation using ModelSim
  • Measuring the performance of your design

• Start now!

• Due: this Thursday
Lab 2: Datapath elements

- Implementing the datapath elements required for a subset of MIPS instructions
- We will give you the design and some other key components
- You will implement the design
- Due 8/16
Lab 3: Lights of life...

- Add control path to Lab 2
- Test your simple processor
- Execute simple programs
- Due on 8/23
Lab 4: It lives!

- Add missing pieces of MIPS
- You know how to have a working processor!
- Due 8/30
Lab 5: Let it live better!

• Pipeline your processor
• Measure the performance
• Due 9/6
Lab 6: Make it awesome!

- Optional
- You can implement any other fancy features in your processor to get an A+
  - Cache
  - Dual-core
  - Branch predictor
  - Speculation
  - Dynamic execution
  - and etc...
Lab space and software

• We will use Altera tools for development (Quartus II)
  • Verilog editing
  • Design analysis
• We will use ModemSim for simulation
  • Simulation
  • Debugging
• Tools are huge pains
• The labs in the CSE basement have the tools installed
  • CSE B250-B270
• They are also available for free
Do the work

- Lab 1 is done independently
- Lab 2-5 should be in group of 2 or 3
  - Choose your group carefully
  - You cannot merge groups
  - Splitting up is allowed
Grading

- Do a reasonable job on the labs (at least a C)
- Delivering a working pipelined processor (A)
- Delivering a working pipelined processor with fancy features (A+)
Staff

• Instructor: Hung-Wei Tseng
  • Lectures: W 6:00p-, WLH 2111
  • Lab hours: TuTh 3:30-4:30p @ CSE B250-B270
    or by appointment
• TA: Mark Gahagan
  • Lab hours: MW 3:30p-6p, Tu 3:30p-6:30p @ CSE B250-B270
• TA: Michael Goldberg
  • Lab hours: MW 11a-1p, Th 3:30p-7:30p @ CSE B250-B270
• Course webpage:
  http://cseweb.ucsd.edu/classes/su12/cse141L-a/
• Discussion board, reading quizzes:
  https://csemoodle.ucsd.edu/course/view.php?id=189
Q & A