CSE140 Week 6 Discussion

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Outline

• Finite State Machines
• Timing and Retiming
Mealy and Moore Machines

- Mealy Machine: general
  - $y_i(t) = f_i(X(t), S(t))$
- Moore Machine: Output is independent of current input
  - $y_i(t) = f_i(S(t))$
  - $S_i(t + 1) = g_i(X(t), S(t))$
- How to convert Mealy to Moore machine?
Implementation

✓ Given: State diagram

   Circuit implementation?
   
   o Example: Lec8 and HW3 “pattern recognizer”

✓ Given: Circuit implementation

   Input output relation?
Implementation

✓ Given: State diagram
  • Derive the state table and assign states
  • Excitation table
  • Equations (K-maps if needed)
  • Circuit implementation
Examples: given a state diagram

- **Step 1: Derive state table and assign states**

  - **Table:**

    | PS/Input | \( X = 0 \) | \( X = 1 \) |
    |---------|-------------|-------------|
    | \( S_0 \) | \( S_0, 0 \) | \( S_1, 0 \) |
    | \( S_1 \) | \( S_0, 0 \) | \( S_2, 0 \) |
    | \( S_2 \) | \( S_0, 1 \) | \( S_2, 0 \) |

- **Assignments:**
  - \( S_0 \Rightarrow 00 \)
  - \( S_1 \Rightarrow 01 \)
  - \( S_2 \Rightarrow 10 \)
Examples: given a state diagram

- **Step 2: Excitation table**
  - $S_0 \Rightarrow 00$
  - $S_1 \Rightarrow 01$
  - $S_2 \Rightarrow 10$

<table>
<thead>
<tr>
<th>PS/Input</th>
<th>$X = 0$</th>
<th>$X = 1$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_0$</td>
<td>$S_0,0$</td>
<td>$S_1,0$</td>
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<td>$S_1$</td>
<td>$S_0,0$</td>
<td>$S_2,0$</td>
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<td>$S_2$</td>
<td>$S_0,1$</td>
<td>$S_2,0$</td>
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</tbody>
</table>

- **Excitation table**

<table>
<thead>
<tr>
<th>$Q_1(t)$</th>
<th>$Q_0(t)$</th>
<th>$X(t)$</th>
<th>$Q_1(t + 1)$</th>
<th>$Q_0(t + 1)$</th>
<th>$y$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
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</tbody>
</table>
Examples: given a state diagram

- **Step 3:** Derive equations
  - Use *D Flip-Flop*: $Q(t+1) = D(t)$
  - K-maps

<table>
<thead>
<tr>
<th>$X(t)/Q_1(t)Q_0(t)$</th>
<th>00</th>
<th>01</th>
<th>11</th>
<th>10</th>
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<tbody>
<tr>
<td>0</td>
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$$D_1(t) = X(t)Q_0(t) + X(t)Q_1(t)$$
Examples: given a state diagram

**Step 3:** Derive equations
- Use D Flip-Flop: $Q(t+1) = D(t)$
- K-maps

\[
D_0(t) = X(t)Q'_0(t)Q'_1(t)
\]

\[
X(t)/Q_1(t)Q_0(t) \quad 00 \quad 01 \quad 11 \quad 10
\]

\[
\begin{array}{cccc}
0 & 0 & 0 & X \\
1 & 1 & 0 & X \\
\end{array}
\]

\[
y = X'(t)Q_1(t)
\]

\[
\begin{array}{cccccc}
Q_1(t) & Q_0(t) & X(t) & Q_1(t + 1) & Q_0(t + 1) & y \\
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 & 1 & 0 \\
0 & 1 & 0 & 0 & 0 & 0 \\
0 & 1 & 1 & 1 & 0 & 0 \\
1 & 0 & 0 & 0 & 0 & 1 \\
1 & 0 & 1 & 1 & 0 & 0 \\
1 & 1 & 0 & X & X & X \\
1 & 1 & 1 & X & X & X \\
\end{array}
\]

\[
D_0(t) \quad output
\]
Examples: given a state diagram

- **Step 4: Circuit implementation**
  - Use D Flip-Flop: \( Q(t+1) = D(t) \)

\[
\begin{align*}
D_1(t) &= X(t)Q_0(t) + X(t)Q_1(t) \\
D_0(t) &= X(t)Q_0'(t)Q_1'(t) \\
y(t) &= X'(t)Q_1(t)
\end{align*}
\]
Implementation

✓ Given: Circuit implementation
   • Excitation table
   • Identify states and derive a state table
   • State diagram
   • Input output relation
Example: given a circuit implementation

• **Step 1:** Excitation table

4. (Finite State Machine Specification) Analyze the following circuit.

4.1 Write the transition (excitation) table (8 points).

• **D Flip-Flop:** $Q(t+1) = D(t)$
  - $D(t)$ can be found with current input $X(t)$ and current state $Q_0(t)$, $Q_1(t)$
Examples : given a circuit implementation

• **Step 1: Excitation table**
  
  o **State Equations**

  \[
  Q_0(t + 1) = XQ_1(t) + XQ_0(t)'
  \]

  \[
  Q_1(t + 1) = XQ_1(t) + XQ_0(t)
  \]

  \[
  M = X'Q_1(t)Q_0(t)
  \]

  o **Excitation table**

<table>
<thead>
<tr>
<th>(Q_1(t))</th>
<th>(Q_0(t))</th>
<th>(X)</th>
<th>(Q_1(t+1))</th>
<th>(Q_0(t+1))</th>
<th>(M)</th>
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</table>
Examples: given a circuit implementation

• Step 2: Identify states and derive state table

  o $S_0 \leftarrow 00$
  $S_1 \leftarrow 01$
  $S_2 \leftarrow 10$
  $S_3 \leftarrow 11$

<table>
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<tbody>
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<td>$S_0,0$</td>
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<td>$S_0,1$</td>
<td>$S_3,0$</td>
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<table>
<thead>
<tr>
<th>$Q_1(t)$</th>
<th>$Q_0(t)$</th>
<th>$X$</th>
<th>$Q_1(t + 1)$</th>
<th>$Q_0(t + 1)$</th>
<th>$M$</th>
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</table>
Examples: given a circuit implementation

• Step 3: State diagram

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<td>$S_0,1$</td>
<td>$S_3,0$</td>
</tr>
</tbody>
</table>
Examples: given a circuit implementation

• Step 4: Input output relation

<table>
<thead>
<tr>
<th>cycle</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
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<th>10</th>
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</thead>
<tbody>
<tr>
<td>$X$</td>
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<td>1</td>
<td>0</td>
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<td>0</td>
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<tr>
<td>state</td>
<td>$S_0$</td>
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</table>

<table>
<thead>
<tr>
<th>cycle</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
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<th>10</th>
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<tr>
<td>$X$</td>
<td>1</td>
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<td>1</td>
<td>0</td>
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<td>0</td>
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<tr>
<td>state</td>
<td>$S_0$</td>
<td>$S_1$</td>
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<td>$M$</td>
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</table>
Sequential Networks: Timing Constraint (without skew)

• Setup Time Constraint

\[ T_c \geq t_{pcq} + t_{pd} + t_{setup} \]

• Hold Time Constraint

\[ t_{ccq} + t_{cd} \geq t_{hold} \]
Sequential Networks: Timing Constraint (with skew)

- **Time Skew**
  - Difference between two clock edges
  - $t_{skew} = CLK2 - CLK1$

- **Setup Time Constraint**
  - CLK2 is earlier than CLK1 ($t_{skew} < 0$)
  
  \[
  T_c \geq t_{pcq} + t_{pd} + t_{setup} - t_{skew}
  \]

- **Hold Time Constraint**
  - CLK2 is later than CLK1
  
  \[
  t_{ccq} + t_{cd} > t_{hold} + t_{skew}
  \]
Example: Timing

- Propagation delay and contamination delay

  ✅ Adder
  - $C_{\text{in}}$ to $C_{\text{out}}/S$
    - $t_{pd} = 20\text{ps}$
    - $t_{cd} = 15\text{ps}$
  - $A/B$ to $C_{out}$
    - $t_{pd} = 25\text{ps}$
    - $t_{cd} = 22\text{ps}$
  - $A/B$ to $S$
    - $t_{pd} = 30\text{ps}$
    - $t_{cd} = 22\text{ps}$

  ✅ D-FF
  - $t_{pcq} = 35\text{ps}$
  - $t_{ccq} = 25\text{ps}$
  - $t_{\text{setup}} = 30\text{ps}$
  - $t_{\text{hold}} = 10\text{ps}$

Maximum frequency?

Figure 2: A four-bit addition machine.
Example: Timing (Without Clock Skew)

- Find the longest path of combinational logic
  \[ t_{pd(max)} = 3 \times t_{pd(c_{in} to c_{out})} + t_{pd(A,B to c_{out})} \]

- Setup Time Constraint
  \[ T_c \geq t_{pcq} + t_{pd} + t_{setup} \]
  \[ T_c \geq (35 + 3 \times 20 + 25 + 30) = 150\text{ps} \]
  the maximum frequency \( \frac{1}{T} = 6.67\text{GHz} \)

- Hold Time Constraint
  \[ t_{cd(min)} = t_{cd(c_{in} to S)} = 15\text{ps} \]
  \[ t_{ccq} + t_{cd(min)} = 25 + 15 = 40\text{ps} \geq t_{\text{hold}} \]
  \[ = 10\text{ps} \]

Figure 2: A four-bit addition machine.
Example: Timing (With Clock Skew)

- Hold Time Constraint
  \[ t_{ccq} + t_{cd(min)} = 25 + 15 = 40\, \text{ps} \]
  \[ \geq t_{\text{hold}} + t_{\text{skew}} = (10 + \Delta)\, \text{ps} \]
  \[ t_{\text{skew}} = 30\, \text{ps} \]
  CLK2 Later than CLK1 !!!

- Setup Time Constraint
  \[ T_c + t_{\text{skew}} \geq t_{\text{pcq}} + t_{\text{pa}} + t_{\text{setup}} \]
  \[ T_c \geq (150 - 30) = 120\, \text{ps} \]
  the maximum frequency \[ \frac{1}{T} = 8.33\, \text{GHz} \]

Figure 2: A four-bit addition machine.