CSE 140 Lecture 13
System Designs

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System Designs

• Introduction
  – Methodology and Framework
• Components
• Specification
• Implementation
Introduction

• Methodology
  • Approach with success stories.
  • Hierarchical designs with interface between the modules (BSV).

• Data Subsystem and Control Subsystem
  • For n-bit data, each operation takes n times or more in hardware complexity.
  • Data subsystem carries out the data operations and transports.
  • Control system sequences the data subsystem and itself.
I. Introduction: Framework

Data Subsystem

Control Subsystem

Data Inputs

Control Inputs

Data Outputs

Control Outputs

Conditions

Control Signals

n=64

Start/Request

Done/Acknowledgement

n=64

Data Subsystem

Control Subsystem
## II. Components

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II. Data Subsystem Components

- Storage: Register, RAM, FIFO, LIFO, Counter, Shifter
- Operator: ALU, Floating Point Operators
- Interconnect: Wire, Buses, Crossbars
II. Components: Storage Modules, Register

LD: Load
CLR: Clear

Q(t+1) = (0, 0, .. , 0) if CLR = 1
     = D         if LD = 1 and CLR = 0
     = Q(t)      if LD = 0 and CLR = 0
Modulo-$n$ Counter

\[
Q(t+1) =
\begin{cases}
(0, 0, \ldots, 0) & \text{if CLR} = 1 \\
D & \text{if LD} = 1 \text{ and CLR} = 0 \\
(Q(t)+1) \mod n & \text{if LD} = 0, \text{ CNT} = 1 \text{ and CLR} = 0 \\
Q(t) & \text{if LD} = 0, \text{ CNT} = 0 \text{ and CLR} = 0
\end{cases}
\]

\[
TC =
\begin{cases}
1 & \text{if } Q(t) = n-1 \text{ and CNT} = 1 \\
0 & \text{otherwise}
\end{cases}
\]
III. Specification: Program

1. Objects (Registers, Outputs of combinational logic)
2. Operation (Logic, Add, Multiplication, DSP, and etc.)
3. Assignment
4. Sequencing

Example:

Signal S1, S2, R[15:0]: FFs, Registers, wires
Z $\leftarrow A + B$: Registers, Adder, Interconnect
R1 $\leftarrow R2$: Registers and Interconnect
Begin, End: Control
if ( ) then ( ), ENDIF: Control
Ex. If C then R1 \(\leftarrow\) S1
Else R2 \(\leftarrow\) S2
Endif;

If C1 then X \(\leftarrow\) A
Else X \(\leftarrow\) B + C
Endif
If C2 then G \(\leftarrow\) X
Endif
VI. Implementation

- Example
- Handshaking
  - Request and Acknowledgement
- Datapath Subsystem
  - Data Operators
  - Data Transporters
- Control Subsystem
  - One Hot Machine Design
VI. Implementation: Example

AddModule(X, Y, Z, start, done)

{ Input X[15:0], Y[15:0] type bit-vector,
  start type boolean;
  Local-Object A[15:0], B[15:0] type bit-vector;
  Output Z[15:0] type bit-vector,
  done type boolean;
  S0: If start’ goto S0 || done ← 1;
  S1: A ← X || B ← Y || done ← 0;
  S2: Z ← Add(A, B) || goto S0;
}

Exercise: Go through the handshaking, data subsystem and control subsystem designs.
AddModule(X,Y,start,done)
Hand Shaking

start

done

\[ t \]
How many clock cycles does the AddModule take to complete one handshaking iteration?
A. One cycle
B. Two cycles
C. More than two cycles
Logistics: Grading

Grade on style, completeness and correctness

- zyBook exercises: 20%
- iClicker: 9% (by participation up to three quarters of classes)
- Homework: 15% (grade based on a subset of problems. If more than 85% of class fill out CAPE evaluations, the lowest homework score will be dropped)
- Midterm 1: 27% (T 5/2/17)
- Midterm 2: 28% (Th 6/8/17)
- Final: 1% (take home exam, due 10PM, Th 6/15/17)

Grading: The best of the following

- The absolute: A- >90% ; B- >80% of total 100% score
- The curve: (A+,A,A-) top 33+ε% of class; (B+,B,B-) second 33+ε%
- The bottom: C- above 45% of absolute score.
Logistics

Grade on style, completeness and correctness

• zyBook exercises: 20% (Half of the points will be added for exercises that missed the due date but are completed by 6/11)
• iClicker: 9% (the points are prorated and saturate up to three quarters of classes)
• HW5 solution will posted asap. Thus, there will be no time for late submission.
• New office hrs for W10 will be posted on the web.
• No discussion session for W10.
• Review session (note for Sunday 6/4, session starts after 2PM)
  – A. Saturday 6/3
  – B. Sunday 6/4