

Name \_\_\_\_\_

**CSE140 Midterm 3, Thursday December 11, 2014**

Please read the following instructions carefully:

If you are unclear about any of the questions on the exam, please make the most plausible assumption to answer the question. Instructors and proctors will not answer questions on the exam material. Please write your name on the top of each page. Write the names of the students to your left and right in the space provided.

Name of student to your left: \_\_\_\_\_

Name of student to your right: \_\_\_\_\_

	Total Points	Points Awarded
Problem I	25	
Problem II	20	
Problem III	25	
Problem IV	30	
Total	100	

Please note that cheating on the exam will have serious consequences.

Don't risk your academic career.

**All the Best!!**



I.2. How much clock skew can the circuit tolerate before it experiences a hold time violation?

$$t_{ccq} + t_{cd} \geq t_{skew} + t_{hold}$$
$$t_{skew} \leq 20ps + 15ps - 30ps = 5ps$$

12 pts for the correct answer.

- 6pts for the correct formula;
- 4pts for correctly substituting values into formula;
- 2pts for obtaining the correct final solution.

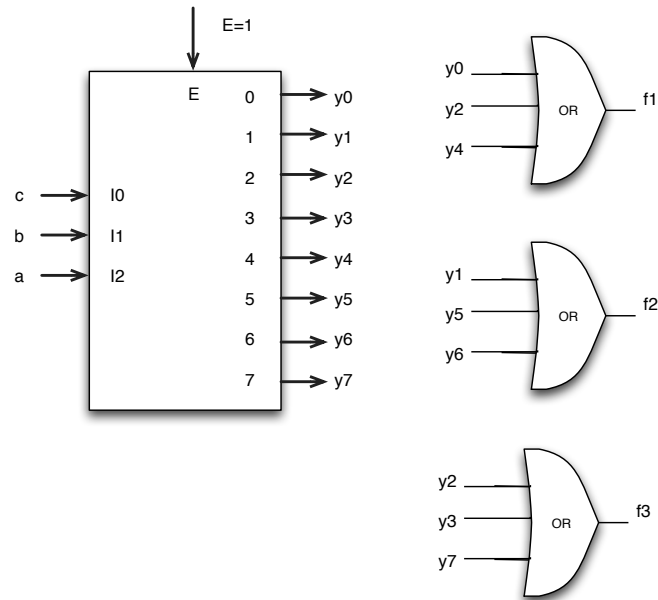
(II) (Decoders) Given three three-input Boolean functions (20 points)

$$f_1(a, b, c) = \sum m(0, 2, 4) + \sum d(1, 6),$$

$$f_2(a, b, c) = \sum m(1, 5, 6),$$

$$f_3(a, b, c) = \sum m(2, 3, 7) + \sum d(1, 5).$$

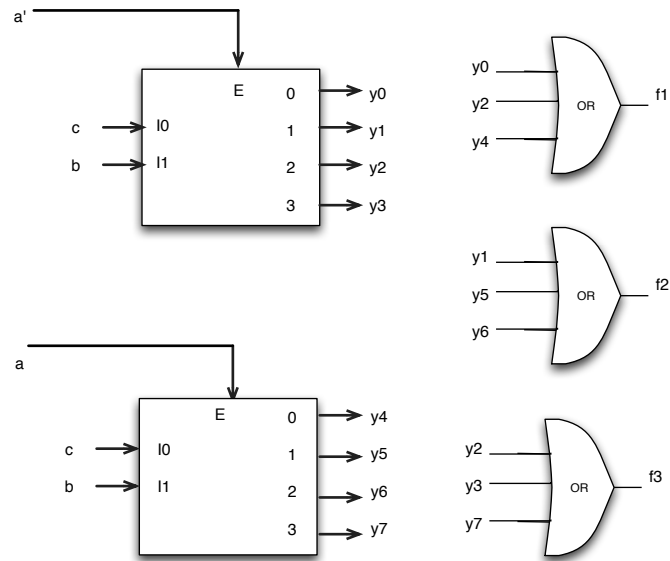
II.1. Implement the functions using a minimal network of 3:8 decoders and OR gates.



Total: 10 pts

- -1pt for no or incorrect labeling
- -1pt for each wrong decoder inputs (lack of input or having additional input variables like  $d$ )
- -4pts for using more than 1 decoder or design does not yield correct output
- -3pts for not connecting the output to each of the three functions

II.2. Implement the functions using a minimal network of 2:4 decoders and OR gates.



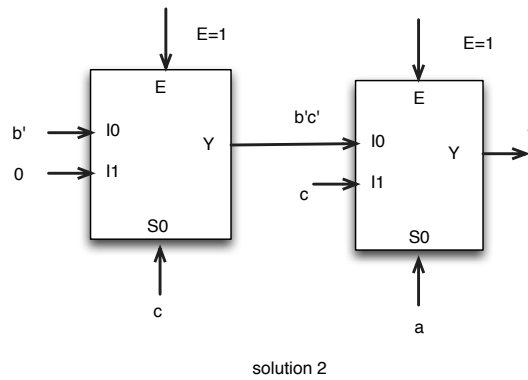
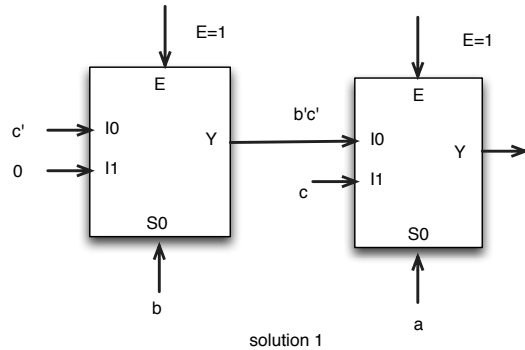
Total: 10 pts

- -1pt for no label or incorrect labeling
- -1pt for each incorrect input to each decoder.
- -3pts not connecting the output to each of the three functions
- -5pts if design is completely different from standard solution for incorrect decoder design. Example, using 3 to 8 decoders or 1 to 2 decoders, or strange design (mixture of decoder and OR gates) that yield incorrect output.
- 1pt for trying, when there is only a truth table or k-map but nothing else.

(III) (Multiplexers) Given a three-input Boolean function (25 points)

$$f(a, b, c) = \sum m(0, 5, 7) + \sum d(3, 6).$$

Implement the function using a minimal network of 2:1 multiplexers by drawing the logic diagram



Total: 25 pts. There are many possible solutions. If final diagram is right, it is full points.  
When the diagram is not correct:

- 2pts for the truth table.
- 3pts for the control signal at table.
- -2pts for one incorrect input of module.

(IV). (System Designs) Implement the following algorithm:

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Alg(X, Y, Z, start, W, done);
Input X[7:0], Y[7:0], Z[7:0], start;
Output W[7:0], done;
Local-object A[7:0], B[7:0], C[7:0];
S0: If start' goto S0 || done  $\leftarrow$  1;
S1: A  $\leftarrow$  X || B  $\leftarrow$  Y || C  $\leftarrow$  Z || done  $\leftarrow$  0;
S2: if (B>A) goto S4;
S3: A  $\leftarrow$  A-B;
S4: if C'[7] goto S2 || C  $\leftarrow$  Inc(C);
S5: A  $\leftarrow$  A-C;
S6: W  $\leftarrow$  A || done  $\leftarrow$  1 || goto S0;
End Alg

```

IV.1. Design a data subsystem that is adequate to execute the algorithm by answering the following questions. (15 points)

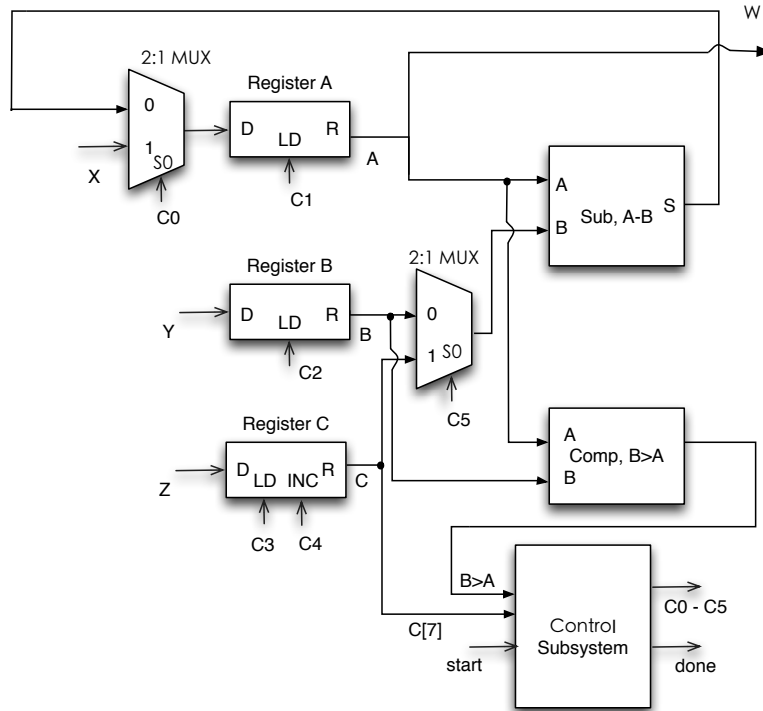
IV.1.1. Use a table to list the instructions and the corresponding components that should be used in the data path subsystem.

State	Statement	Operation	Control Signal
S1	A $\leftarrow$ X	A $\leftarrow$ Load(X)	C0=1, C1=1
S1	B $\leftarrow$ Y	B $\leftarrow$ Load(Y)	C2=1
S1	C $\leftarrow$ Z	C $\leftarrow$ Load(Z)	C3=1
S2	B>A	Comp(A,B)	
S3	A $\leftarrow$ A-B	A $\leftarrow$ Sub(A,B)	C0=0, C1=1
S4	C $\leftarrow$ Inc(C)	C $\leftarrow$ Inc(C)	C4=1
S5	A $\leftarrow$ A-C	A $\leftarrow$ Sub(A,C)	C0=0, C1=1, C5=1
S6	W $\leftarrow$ A	wire	done=1

Total: 8 pts. Here, the column of control signal is not required.

- -1pt for wrong row (any mistake within the row).

IV.1.2. Draw the schematic diagram to show the data path subsystem. Label the inputs, outputs, and control signals of all components.



Total: 7 pts. There are many possible solutions. Go through the design. If the design is correct, it is full points.

- -1pt for missing one module.
- -1pt for a wrong wire.
- up to -3pts for the missing or wrong control subsystem.
- -1pt for one wrong input into control subsystem.



IV.2. Design the control subsystem by answering the following questions. (15 points)

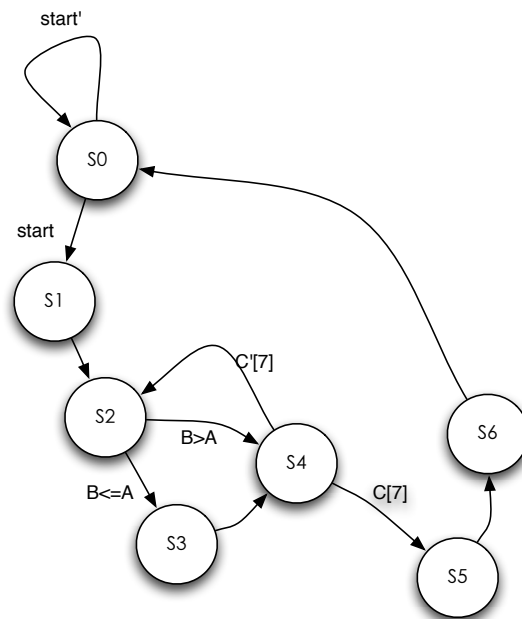
IV.2.1. Use a table to list the value of control signals for every state.

State	C0 (mux1)	C1 (Reg A)	C2 (Reg B)	C3 (Reg C LD)	C4 (Reg C Inc)	C5 (mux2)	done
S0	0	0	0	0	0	0	1
S1	1	1	1	1	0	0	0
S2	-	0	0	0	0	0	0
S3	0	1	0	0	0	0	0
S4	-	0	0	0	1	0	0
S5	0	1	0	0	0	1	0
S6	-	0	0	0	0	0	1

Total: 5 pts. The table depends on IV.1's design.

- -0.5pt for wrong row (any mistake within the row).

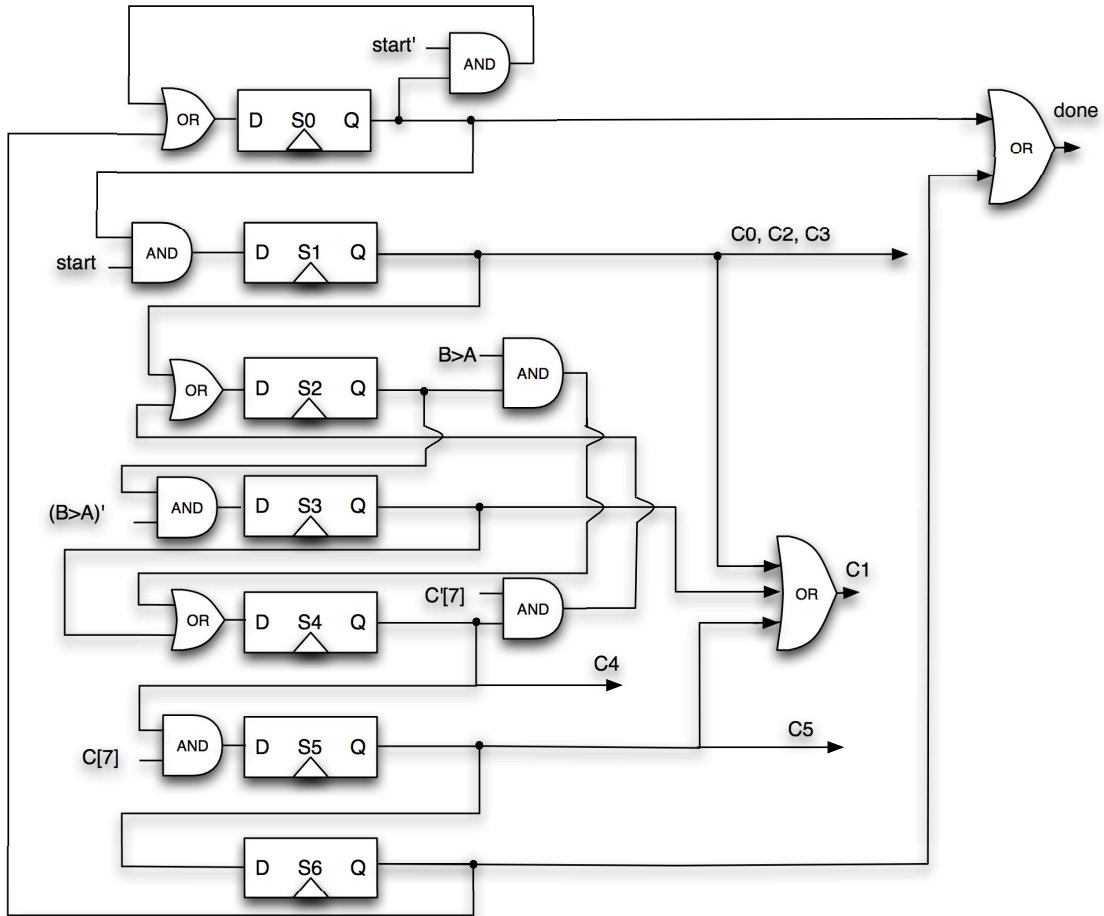
IV.2.2. Draw the state diagram.



Total: 5 pts.

- -0.5pt for wrong state/label.

IV.2.3. Implement the control subsystem using a one hot encoding design. Draw the logic diagram.



Total: 5 pts.

- -1pt for missing one AND gate.
- -1pt for missing one OR gate (the inputs of flip-flop).
- -1pt for no control and -0.5pt for a small mistake on the control