Performance

Hung-Wei Tseng
Instruction set architecture

• Defines the language that your processor should speak
• Provides an abstraction for software to access hardware functions
  • Arithmetic operations: add, sub, mul, div
  • Logical operations: and, or, not
  • Memory access: load, store
  • Control: branch, jump
## MIPS v.s. x86

<table>
<thead>
<tr>
<th></th>
<th>MIPS</th>
<th>x86</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISA type</td>
<td>RISC</td>
<td>CISC</td>
</tr>
<tr>
<td>instruction width</td>
<td>32 bits</td>
<td>1 ~ 17 bytes</td>
</tr>
<tr>
<td>code size</td>
<td>larger</td>
<td>smaller</td>
</tr>
<tr>
<td>registers</td>
<td>32</td>
<td>16</td>
</tr>
<tr>
<td>addressing modes</td>
<td>reg+offset</td>
<td>base+offset, base+index,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>scaled+index, scaled+index+</td>
</tr>
<tr>
<td></td>
<td></td>
<td>offset</td>
</tr>
<tr>
<td>hardware</td>
<td>simple</td>
<td>complex</td>
</tr>
</tbody>
</table>
Announcement

- Homework #1 due next Tuesday
  - Tutor hours tomorrow 3p-5p
  - One more TA -- Harsha Basavaraj (Friday 1p-2p @CSE B260A)
  - Check google calendar http://goo.gl/JJyrXp
- Reading quizzes due next Thursday
- The system of achievements
  - You get one bonus point when you give a “good” answer
  - You can only get at most one bonus point in this quarter
  - A “good” answer doesn’t have to be “right” answer. Especially many answers can change in technology evolutions.
  - I will give priority to those who never answer a question before
  - You will get a special prize from me if you’re one of the top 3 who answered the most questions!
Outline

• What is performance?
• What is the performance equation?
• What affects performance
• Amdahl’s Law
Performance!
What do you want in a computer?

- Frame rate
- Responsiveness
- Real-time
- Throughput
- Cost
- Volume
- Weight
- Battery life
- Low power/low temperature
- Reliability
- Latency/Execution time

The most direct measurement of performance.
Execution Time

- The simplest kind of performance
- Shorter execution time means better performance
- Usually measured in seconds

How many of these? Instruction Count!

How long is it take to execution each of these? Cycles per instruction * cycle time

Instruction memory

<table>
<thead>
<tr>
<th>Address</th>
<th>Opcode</th>
<th>Operation</th>
<th>Register(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>120007a30</td>
<td>0f00bb27</td>
<td>ldah gp,15(t12)</td>
<td></td>
</tr>
<tr>
<td>120007a34</td>
<td>509cbd23</td>
<td>lda gp,-25520(gp)</td>
<td></td>
</tr>
<tr>
<td>120007a38</td>
<td>00005d24</td>
<td>ldah t1,0(gp)</td>
<td></td>
</tr>
<tr>
<td>120007a3c</td>
<td>0000bd24</td>
<td>ldah t4,0(gp)</td>
<td></td>
</tr>
<tr>
<td>120007a40</td>
<td>2ca422a0</td>
<td>ld1 t0,-23508(t1)</td>
<td></td>
</tr>
<tr>
<td>120007a44</td>
<td>130020e4</td>
<td>beq t0,120007a94</td>
<td></td>
</tr>
<tr>
<td>120007a48</td>
<td>00003d24</td>
<td>ldah t0,0(gp)</td>
<td></td>
</tr>
<tr>
<td>120007a4c</td>
<td>2ca4e2b3</td>
<td>stl zero,-23508(t1)</td>
<td></td>
</tr>
<tr>
<td>120007a50</td>
<td>0004ff47</td>
<td>clr v0</td>
<td></td>
</tr>
<tr>
<td>120007a54</td>
<td>28a4e5b3</td>
<td>stl zero,-23512(t4)</td>
<td></td>
</tr>
<tr>
<td>120007a58</td>
<td>20a421a4</td>
<td>ldq t0,-23520(t0)</td>
<td></td>
</tr>
<tr>
<td>120007a5c</td>
<td>0e0020e4</td>
<td>beq t0,120007a98</td>
<td></td>
</tr>
<tr>
<td>120007a60</td>
<td>0204e147</td>
<td>mov t0,t1</td>
<td></td>
</tr>
<tr>
<td>120007a64</td>
<td>0304ff47</td>
<td>clr t2</td>
<td></td>
</tr>
<tr>
<td>120007a68</td>
<td>0500e0c3</td>
<td>br 120007a80</td>
<td></td>
</tr>
</tbody>
</table>
Performance equation!
Performance Equation

Execution Time = \frac{\text{Instructions}}{\text{Program}} \times \frac{\text{Cycles}}{\text{Instruction}} \times \frac{\text{Seconds}}{\text{Cycle}}

- How many instructions executed?
- How long is it to execute each instruction?

- ET = IC * CPI * CT
- IC (Instruction Count)
- CPI (Cycles Per Instruction)
- CT (Seconds Per Cycle)
- 1 Hz = 1 second per cycle; 1 GHz = 1 ns per cycle
Performance Example

• Assume that we have an application composed with a total of **500000** instructions, the average CPI of the application is **2** cycle. If the processor runs at **1GHz**, how long is it take to execution the application?

A. 500000 ns  
B. 1000000 ns  
C. 1750000 ns  
D. 3500000 ns  
E. None of the above

**Execution Time** = \( \frac{\text{Instructions}}{\text{Program}} \times \frac{\text{Cycles}}{\text{Instruction}} \times \frac{\text{Seconds}}{\text{Cycle}} \)

\[500000 \times 2 \times 1 \text{ ns} = 1000000 \text{ ns}\]
### Performance Example

- Assume that we have an application composed with a total of 500000 instructions, in which 20% of them are the load/store instructions with an average CPI of 6 cycles, and the rest instructions are integer instructions with average CPI of 1 cycle. If the processor runs at 1GHz, how long is the execution time?

<table>
<thead>
<tr>
<th>Option</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>A.</td>
<td>500000 ns</td>
</tr>
<tr>
<td>B.</td>
<td>1000000 ns</td>
</tr>
<tr>
<td>C.</td>
<td>1750000 ns</td>
</tr>
<tr>
<td>D.</td>
<td>3500000 ns</td>
</tr>
<tr>
<td>E.</td>
<td>None of the above</td>
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</table>

**Execution Time** = \( \frac{\text{Instructions}}{\text{Program}} \times \frac{\text{Cycles}}{\text{Instruction}} \times \frac{\text{Seconds}}{\text{Cycle}} \)

\[
500000 \times (0.8 \times 1 + 0.2 \times 6) \times 1 \text{ ns} = 1000000 \text{ ns}
\]
Speedup

• Compare the relative performance of the baseline system and the improved system

• Definition

\[
\text{Speedup} = \frac{\text{Execution time}_{\text{baseline}}}{\text{Execution time}_{\text{improved system}}}
\]
Performance Example

- Assume that we have an application composed with a total of 500000 instructions, in which 20% of them are the load/store instructions with an average CPI of 6 cycles, and the rest instructions are integer instructions with average CPI of 1 cycle.
- If we double the clock rate to 2GHz without improving the memory latency, the average CPI for load/store instruction will also become 12 cycles. What’s the performance improvement after this change?
  
  A. No change
  B. 1.25
  C. 1.5
  D. 2
  E. None of the above
Performance Example

- Assume that we have an application composed with a total of 500000 instructions, in which 20% of them are the load/store instructions with an average CPI of 6 cycles, and the rest instructions are integer instructions with average CPI of 1 cycle.
- If we double the clock rate to 2GHz without improving the memory latency, the average CPI for load/store instruction will also become 12 cycles. What’s the performance improvement after this change?

\[
\text{Execution Time} = \frac{\text{Instructions}}{\text{Program}} \times \frac{\text{Cycles}}{\text{Instruction}} \times \frac{\text{Seconds}}{\text{Cycle}}
\]

\[
ET_{\text{new}} = 500000 \times (0.8\times1 + 0.2\times12) \times 0.5 \text{ ns} = 800000 \text{ ns}
\]

\[
\text{Speedup} = \frac{ET_{\text{old}}}{ET_{\text{new}}} = \frac{1000000}{800000} = 1.25
\]
Identify the performance bottleneck

Why does an Intel Core i7 @ 3.5 GHz usually perform better than an Intel Core i5 @ 3.5 GHz or AMD FX-8350@4GHz?

A. Because the instruction count of the program are different  
B. Because the clock rate of AMD FX is higher  
C. Because the CPI of Core i7 is better  
D. Because the clock rate of AMD FX is higher and CPI of Core i7 is better  
E. None of the above
Why does an Intel Core i7 @ 3.5 GHz usually perform better than an Intel Core i5 @ 3.5 GHz or AMD FX-8350@4GHz?

$ET = \frac{\text{Instructions}}{\text{Program}} \times \frac{\text{Cycles}}{\text{Instruction}} \times \frac{\text{Seconds}}{\text{Cycle}}$

- $ET = IC \times CPI \times \text{Cycle Time}$

Every time when the question ask you about the “performance”, thinking about the performance equation first!
What affects performance
What affects performance?

- How many of the following factors affect performance?
  - Compiler
  - Instruction Set
  - Architecture
  - Programmer
  - Application
  - Processor architecture
  - Process technology
  - Programming languages

A. 3
B. 4
C. 5
D. 6
E. 7
How programmer affects performance?

- ET = IC * CPI * CT
- What can a programmer affect?
  A. IC
  B. IC & CPI
  C. IC, CPI & CT
  D. IC & CT
Demo: programmer & performance

- Row-major, column major
- Let’s identify where the performance gain is from!
  - Using “performance counters”
  - You may use “perf stat” in linux
  - You can also create your own functions to obtain counter values
How compiler affects performance?

- $ET = IC \times CPI \times CT$
- What can a compiler affect?
  A. IC
  B. IC & CPI
  C. IC, CPI & CT
  D. IC & CT
Demo: compiler & performance

- Compiler optimization can help reducing the instruction count
- Compiler optimization can improve CPI
  - Wise selection of instruction combinations
  - Use registers to eliminate loads and stores
Demo: storage and performance

- Machine implementation affects performance
- The same CPU, but different storage devices
  - Loading data from a H.D.D: access time ~ 10ms
  - Loading data from an S.S.D: access time ~ 100 us
Summary: Performance Equation

Execution Time = \( \frac{\text{Instructions}}{\text{Program}} \times \frac{\text{Cycles}}{\text{Instruction}} \times \frac{\text{Seconds}}{\text{Cycle}} \)

- ET = IC * CPI * Cycle Time
- IC (Instruction Count)
  - ISA, Compiler, algorithm, programming language
- CPI (Cycles Per Instruction)
  - Machine Implementation, microarchitecture, compiler, application, algorithm, programming language
- Cycle Time (Seconds Per Cycle)
  - Process Technology, microarchitecture, programmer