Lecture 10:
Sequential Networks: Timing and Retiming

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Timing

• Clock specifies a precise time for the next state
• Too late: fail to reach for the setup of the next state.
• Too early: Race to disturb the holding of the next state.
• Analysis: Verify the timing of the system.
• Goal: A robust design.
A typical sequential network has combinational circuit between registers (R1 to R2). The registers are synchronized by clocks (CLK1 to CLK2). Timing is set between clocks (CLK1 and CLK2).
\[ t_{cq} + t_{comb} + t_{setup} \leq T \]
\[ t_{hold} < t_{cq} + t_{comb} \]

- \( t_{cq} \): time from rising edge of clock to Q update (CLK1⇒B)
- \( t_{comb} \): time of combinational logic delay (B⇒C)
- \( t_{setup} \): setup time before rising edge of clock (C⇒CLK2)
- \( t_{hold} \): hold time after the rising edge of clock
- \( T \): clock period (CLK1⇒CLK2)
So far ....

Combinational

CLK
• When does our (seemingly logically correct) design go wrong?

• How can we design a circuit that works under real constraints?
Timing Constraints of flip flops

Q: What is the output of the flip flop at time $t_1$?

A. One  
B. Zero  
C. Can’t say for sure
Timing Constraints of flip flops

What if the input transition happens late, close to the rising edge?
A. Output will still be one at $t_1$
B. Output will be zero at $t_1$
C. Can’t say for sure
Input Timing Constraint: Set up time

I. Setup time: $t_{\text{setup}}$

This is the time before the clock edge that data must be stable (i.e. not change)
I. Is it okay for the input to the flip flop to change right after the rising edge?
Input Constraints: Set up and hold time

I. Setup time: $t_{\text{setup}}$
   Time before the clock edge that data must be stable (i.e. not change)

II. Hold time: $t_{\text{hold}}$
   Time after the clock edge that data must be stable

Aperture time: $t_a$
Time around clock edge that data must be stable ($t_a = t_{\text{setup}} + t_{\text{hold}}$)
I. Setup time violation

This occurs if the input data signal does not remain unchanged for at least $t_{\text{setup}}$ before the clock edge.

II. Hold time violation

This occurs if the input data signal does not remain unchanged for at least $t_{\text{setup}}$ after the clock edge
Output Timing Constraints

CLK

Q

Q'

\( t_{ccq} \)

\( t_{pcq} \)
Output Timing Constraints

I. Contamination delay: $t_{ccq}$
   Time after clock edge that $Q$ might be unstable (i.e., start changing)

II. Propagation delay: $t_{pcq}$
   Time after clock edge that the output $Q$ is guaranteed to be stable (i.e., to stop changing)
PIQ: A hold time violation is likely to occur when

A. The input signal (into the flip flop) fails to change to a desired value fast enough
B. The output signal (out of the flip flop) takes too long to stabilize
C. The input signal (into the flip flop) does not remain stable long enough after the clock edge
D. The output signal (out of the flip flop) changes too quickly
PIQ: The timing of which of the following signals can cause a setup-time violation?

A. The input signal $T(t)$
B. The output signal $Q(t)$
C. The clock signal, CLK
D. Some of the above: $T(t)$, CLK
E. None of the above
PIQ: For a given flip-flop implementation which of its timing parameters can we modify when designing a sequential network (depicted below)

A. Set up and hold time  
B. Propagation and Contamination delays  
C. All of the above  
D. None of the above

We cannot modify the timing constraints of the flip-flop. We can only ensure that the constraints are met when designing the circuit.
Fact 1: Once a flip flop has been ‘built’ we are stuck with its timing characteristics: $t_{\text{setup}}$, $t_{\text{hold}}$, $t_{\text{ccq}}$, $t_{\text{pcq}}$

Now let’s look at the timing characteristics of the combinational part
Combinational Logic: Output timing constraints

I. Why don’t we have input constraints?

No dead time dictated by the clock
Combinational Logic: Output timing constraints

\[ \begin{align*}
X_1 & \quad Y_1 \\
X_2 & \quad Y_2 \\
X_3 & \quad Y_3 \\
X_4 & \quad Y_4 \\
\end{align*} \]

Combinational circuit

I. Contamination delay: \( t_{cd} \)
   Minimum time from when an input changes until any output \textit{starts} to change
Combinational Logic: Output timing constraints

I. Contamination delay: $t_{cd}$
   Minimum time from when an input changes until any output starts to change

II. Propagation delay: $t_{pd}$
   Maximum time from when an input changes until the output or outputs of a combinational circuit are guaranteed to reach their final value (i.e., stop changing)
Combinational Logic: Output timing constraints

PI Q: Which path in the above circuit determines the contamination delay of the circuit (assuming the delay of all the gates is the same)?

A. AND- OR – NOR
B. AND-OR
C. NOR
D. OR-NOR
PI Q: Which path in the above circuit determines the propagation delay of the circuit (assuming the delay of all the gates is the same)?

A. AND- OR – NOR
B. AND-OR
C. NOR
D. OR-NOR
An alternate view of the sequential circuit
The delay between registers has a **minimum** and **maximum** delay, dependent on the delays of the circuit elements (Dynamic Discipline)

\[
\begin{align*}
\text{min delay for } D_2 & = t_{c_q} (R1) + t_{cd} (CL) \\
\text{max delay for } D_2 \text{ (stable)} & = t_{p_c q} (R1) + t_{pd} (CL)
\end{align*}
\]

Propagating delay of R1.
PI Q: Suppose input to $R_1$ changed before $t_1$, what is the maximum delay (from $t_1$) after which $D_2$ reaches a stable value?

A. Setup time of $R_1$ + Propagation delay of $CL$ + Propagation delay of $R_2$
B. Hold time of $R_1$ + Propagation delay of $CL$ + setup time of $R_1$
C. Propagation delay of $R_1$ + Propagation delay of $CL$ + Propagation delay of $R_2$
D. Propagation delay of $R_1$ + Propagation delay of $CL$
E. Propagation delay of $CL$ + Propagation delay of $R_2$
PI Q: Suppose input to R1 changed before \( t_1 \), what is the minimum delay (from \( t_1 \)) after which D2 starts to change?

A. Setup time of R1 + propagation delay of CL + propagation of R2

B. Hold time of R1 + propagation time of CL + setup time of R1

C. Hold time of R1 + Contamination delay of CL + Propagation time of R2

D. Contamination delay of R1 + Contamination delay of CL

E. Contamination delay of CL + Contamination delay of R2

Only depends on R1 & CL
Setup Time Constraint

- The setup time constraint depends on the maximum delay from register R1 through the combinational logic.
- The input to register R2 must be stable at least $t_{\text{setup}}$ before the clock edge.

Maximum delay, $t_{\text{max}} = t_{\text{pcq}}(R1) + t_{\text{pd}}(CL)$

Setup Time Constraint:

$$t_{\text{max}} + t_{\text{setup}} < T_c$$
Setup Time Constraint

\[ T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}} \]

\[ t_{pd} \leq T_c - (t_{pcq} + t_{\text{setup}}) \]

Parameters we can control:
- \( t_{pcq} \)
- \( t_{pd} \)
- \( t_{\text{setup}} \)

Parameters we cannot control:
- \( T_c \)

Adjust by designing the circuit appropriately.
Hold Time Constraint

- The hold time constraint depends on the **minimum** delay from register R1 through the combinational logic.
- The input to register R2 must be stable for at least $t_{\text{hold}}$ after the clock edge.

Minimum delay, $t_{\text{min}}$

$$t_{\text{min}} = t_{\text{ccq}}(R1) + t_{\text{cd}}(\text{CLK})$$

Hold Time Constraint:

$$t_{\text{min}} > t_{\text{hold}}$$
To understand the hold time constraint, imagine the following scenario:

We need \(D_2\) to remain stable for at least \(\text{hold}\) after the clock edge. However, \(D_2\) can change after the clock edge (Why?)

The input to \(R\), which is \(D_2\), changed from 0 to 1 before the clock edge & remained stable until the clock edge.
$D_2$ can change after the clock edge because $D_2$ is the output of the combinational logic whose input is the output of another flip-flop ($R1$). Since the output of $R1$ can change anytime after the clock edge, that can cause $D_2$ to change after the clock edge.

What is the min time for which $D_2$ is guaranteed to not change after the clock edge?
The min. time for which D₂ is guaranteed to not change after the clock edge is:
the contamination delay of R₁ + the contamination delay of the combinational logic.

If we want D₂ to be stable for at least thold after the clock edge & not get contaminated earlier than that we need:
(Contamination delay (R₁) + Contamination delay (CL)) should be greater than thold.
Hold Time Constraint

\[ t_{\text{hold}} < t_{\text{ccq}} + t_{\text{cd}} \]

\[ t_{\text{cd}} > t_{\text{hold}} - t_{\text{ccq}} \]
Timing Analysis

**Timing Characteristics**

- \( t_{ccq} = 30 \text{ ps} \)
- \( t_{pcq} = 50 \text{ ps} \)
- \( t_{setup} = 60 \text{ ps} \)
- \( t_{hold} = 70 \text{ ps} \)

**Gate**

- \( t_{pd} = 35 \times 3 = 105 \text{ ps} \)
- \( t_{cd} = 25 \text{ ps} \)

**Setup time constraint:**

\[
T_c \geq t_{pcq} + t_{pd}(CL) + t_{setup}
\]

\[
f_c = 1/T_c
\]

**Hold time constraint:**

\[
t_{ccq} + t_{cd} > t_{hold}
\]
Timing Analysis

Timing Characteristics

- \( t_{ccq} = 30 \text{ ps} \)
- \( t_{pcq} = 50 \text{ ps} \)
- \( t_{setup} = 60 \text{ ps} \)
- \( t_{hold} = 70 \text{ ps} \)
- \( t_{pd} = 35 \text{ ps} \)
- \( t_{cd} = 25 \text{ ps} \)

Setup time constraint:

\[ T_c \geq (50 + 105 + 60) \text{ ps} = 215 \text{ ps} \]

\[ f_c = \frac{1}{T_c} = 4.65 \text{ GHz} \]

Hold time constraint:

\[ t_{ccq} + t_{cd} > t_{hold} \]?

\[ (30 + 25) \text{ ps} > 70 \text{ ps} \] ? No!

\[ t_{pd} \times 3 = 3 \times 35 \text{ ps} = 105 \text{ ps} \]
Fixing Hold Time Violation

Add buffers to the short paths:

Timing Characteristics

- $t_{ccq} = 30$ ps
- $t_{pcq} = 50$ ps
- $t_{setup} = 60$ ps
- $t_{hold} = 70$ ps
- $t_{pd} = 35$ ps
- $t_{cd} = 25$ ps

Setup time constraint:

\[ T_c \geq \]

Hold time constraint:

\[ t_{ccq} + t_{cd} > t_{hold} ? \]
Fixing Hold Time Violation

Add buffers to the short paths:

$\begin{aligned}
t_{pd} &= 3 \times 35 \text{ ps} = 105 \text{ ps} \\
t_{cd} &= 2 \times 25 \text{ ps} = 50 \text{ ps}
\end{aligned}$

Setup time constraint:
$T_c \geq (50 + 105 + 60) \text{ ps} = 215 \text{ ps}$

$f_c = 1/T_c = 4.65 \text{ GHz}$

Hold time constraint:
$t_{ccq} + t_{cd} > t_{hold}$?

$(30 + 50) \text{ ps} > 70 \text{ ps}$? Yes!

Timing Characteristics

$\begin{aligned}
t_{ccq} &= 30 \text{ ps} \\
t_{pcq} &= 50 \text{ ps} \\
t_{setup} &= 60 \text{ ps} \\
t_{hold} &= 70 \text{ ps}
\end{aligned}$

$\begin{aligned}
t_{pd} &= 35 \text{ ps} \\
t_{cd} &= 25 \text{ ps}
\end{aligned}$
Clock Skew

- The clock doesn’t arrive at all registers at the same time
- Skew is the difference between two clock edges
- Examine the worst case to guarantee that the dynamic discipline is not violated for any register – many registers in a system!
Setup Time Constraint with Clock Skew

- In the worst case, the CLK2 is earlier than CLK1

\[ T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}} + t_{\text{skew}} \]
\[ t_{pd} \leq T_c - (t_{pcq} + t_{\text{setup}} + t_{\text{skew}}) \]

If the rising edge of CLK2 arrives earlier than CLK1 by \( t_{\text{skew}} \), the time available for DL to stabilize is reduced by \( t_{\text{skew}} \).
Timing Analysis with clock skew

Timing Characteristics

\[
\begin{align*}
  t_{ccq} & = 30 \text{ ps} \\
  t_{pcq} & = 50 \text{ ps} \\
  t_{\text{setup}} & = 60 \text{ ps} \\
  t_{\text{hold}} & = 70 \text{ ps}
\end{align*}
\]

\[
\begin{align*}
  t_{pd} & = 35 \text{ ps} \\
  t_{cd} & = 25 \text{ ps}
\end{align*}
\]

\[t_{pd} = 3 \times 35 \text{ ps} = 105 \text{ ps}\]

\[t_{cd} = 25 \text{ ps}\]

Setup time constraint:

\[
T_c \geq 265 \text{ ps}
\]

\[
f_c = \frac{1}{T_c} = 3.77 \text{ GHz}
\]

Without skew we got \(f_c = 4.65 \text{ GHz}\)
Hold Time Constraint with Clock Skew

- In the worst case, CLK2 is later than CLK1

$t_{ccq} + t_{cd} > t_{hold} + t_{skew}$

$t_{cd} > t_{hold} + t_{skew} - t_{ccq}$
Hold Time Violation

Add buffers to the short paths:

Timing Characteristics

\[
\begin{align*}
  t_{ccq} &= 30 \text{ ps} \\
  t_{pcq} &= 50 \text{ ps} \\
  t_{setup} &= 60 \text{ ps} \\
  t_{hold} &= 70 \text{ ps} \\
  t_{pd} &= 35 \text{ ps} \\
  t_{cd} &= 25 \text{ ps} \\
  t_{skew} &= 50 \text{ ps}
\end{align*}
\]

\[
\begin{align*}
  t_{pd} &= 3 \times 35 \text{ ps} = 105 \text{ ps} \\
  t_{cd} &= 2 \times 25 \text{ ps} = 50 \text{ ps}
\end{align*}
\]

Hold time constraint:

\[
t_{ccq} + t_{cd} > t_{hold} + t_{skew}?
\]

\[
(30 + 50) \text{ ps} > (70 \text{ ps} + 50) \text{ ps}?
\]
Using Clock Skew advantageously (Retiming)

- Suppose CLK2 is later than CLK1 by $t_{skew(1,2)}$

\[
t_{ccq} + t_{cd} > t_{hold} + t_{skew(1,2)}
\]

\[
t_{skew(1,2)} < t_{ccq} + t_{cd} - t_{hold}
\]

\[
T_c + t_{skew(1,2)} \geq t_{pcq} + t_{pd} + t_{setup}
\]
Retiming

Add buffers to the short paths:

\[ t_{pd} = 3 \times 35 \text{ ps} = 105 \text{ ps} \]
\[ t_{cd} = 2 \times 25 \text{ ps} = 50 \text{ ps} \]

\[ t_{skew(1,2)} < t_{ccq} + t_{cd} - t_{hold} \quad (10 \text{ ps}) \]

\[ T_c + t_{skew(1,2)} \geq t_{pcq} + t_{pd} + t_{setup} \quad (215 \text{ ps}) \]
Timing and Retiming

- Retiming: Adjust the clock skew so that the clock period can be reduced.