Verilog Design Examples

Greatest Common Divisor
GCD in C

```c
int GCD(int inA, int inB)
{
    int done = 0;
    int A = inA;
    int B = inB;
    while (!done)
    {
        if (A < B)
        {
            swap = A;
            A = B;
            B = swap;
        }
        else if (B != 0)
        {
            A = A - B;
        }
        else
        {
            done = 1;
        }
    }
    return A;
}
```

What does the RTL implementation need?

- **inputs**
  - State
  - iteration
  - Less-Than Comparator
  - Swap
  - Equal Comparator
  - Subtractor
  - Termination control

Output

Courtesy of Arvind http://csg.csail.mit.edu/6.375/
Design an appropriate port interface

Input_valid_in, input_consumed_out, A_in, B_in, clk, reset

Result_valid_out, Output_consumed_in, Result_out

Courtesy of Arvind http://csg.csail.mit.edu/6.375/
Design a datapath which has the functional units

A = inA; B = inB;
while (!done)
begin
  if (A < B)
    swap = A;
    A = B;
    B = swap;
  else if (B != 0)
    A = A - B;
  else
    done = 1;
End

Y = A;
Datapath module interface
Control unit requires a state machine for valid/ready signals

- **WAIT**
  - Waiting for new input operands
  - Input_valid_in → A_ff_en_out
  - B_zero_in → A_mux_sel_out

- **CALC**
  - Swapping and subtracting
  - B_zero_in → B_mux_sel_out

- **DONE**
  - Waiting for consumer to take the result
  - Result_consumed_in → B_ff_en

Reset
RTL test harness requires proper handling of the ready/valid signals