CSE140: Components and Design Techniques for Digital Systems

Tajana Simunic Rosing
- Total students enrolled: 150
- # Solutions received: 135
- Max score: 100.00
- Min score (w/o 0s): 13.00
- Mean score: 82.00
- Median score: 90.00
Where we are now

• **What we’ve covered so far** (Chap 1 & 2)
  – Number representations
  – CMOS transistor design and delay
  – Boolean algebra
  – SOP and POS, Logic minimization using K-maps
  – Two and multi-level implementation
  – Gate delay and Hazards
  – Mux and Demux

• **Exam on next Thursday**
  – 8 ½ x 11” paper with handwritten notes (both sides)

• **What comes next:**
  – Review for the exam
  – Chapter 3: Sequential circuits
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Review

Tajana Simunic Rosing
CMOS problem

• Implement \( F = ab(c+d) \) in CMOS and calculate min and max delay from inputs to output \( F \) assuming 2\( C_g \) capacitance is at the output
Worst case CMOS delay

• What is the worst case delay and which combination of inputs produces it?
K-maps, Hazards, Muxes

\[ F(A, B, C, D) = \Pi M(2, 3, 6, 8, 9, 12, 13, 14) \]
Mux & Demux

• Implement F using a mux and demux

\[ F(A, B, C, D) = \sum m(2, 4, 7, 9, 10, 11, 14) + \sum d(3, 6, 12) \]
Decoder

• You are given a 2:4 decoder, a 2 input OR gate and a 3 input OR gate. Using these components design a system which takes A & B as inputs and generates the following four outputs: AB, (AB)', A+B, (A+B)'
Conversion to NOR gates

- Use De Morgan’s:
  - $A' + B' = (A \cdot B)'$
  - $A' \cdot B' = (A+B)'$
NAND gates implementation

\[ A = (X + ((\overline{Y})(Z)))(Y + \overline{Z}) \]
Decoder

• Implement $F(A, B, C) = A'C' + AC'$ with a minimum size circuit. You may use a 2:4 decoder and at most one other gate.
Design problem – distance between numbers

- Design a circuit that gives the absolute distance between the two numbers (e.g. $x=3$ $y=1$ $d=2$)

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Hazards

• Minimize F and express the result using maxterms. Is the minimum implementation static-0 hazard free? If not, what term(s) do you need to add to make it static-0 hazard free?
Hazards and delay

• Assuming each gate takes 1 unit delay, is there a hazard on the following transition: 1110 → 1100? What kind of hazard is it?