CSE140 – Spring 2013

CSE140 Homework #2

You must **SHOW ALL STEPS** for obtaining the solution. Reporting the correct answer, without showing the work performed at each step will result in getting 0 points for that problem.

Problems:

**Note:** Problem no’s are from ‘Digital Design and Computer Architecture (2nd Edition)’

1. Problem 1.74

2. Construct using NOR gates only. You may also use inverters.
   \[ F(X,Y, Z) = (X'+Z') (Y+Z) (X+Y'+Z) \]

3a. Estimate the delay in picoseconds \((1\text{ps}=10^{12}\text{ sec})\) to switch output logic state of Inverter Output (Point X) from 0->1 for the circuit shown in figure below. Assume \(R_p=20\text{KOhm}, R_n=10\text{KOhm}\). Input capacitance of all transistors is \(C = 0.5 \text{ fF} \ (1\text{fF} = 10^{15} \text{ F})\).

   (Hint: Estimate delay as \(\Delta T = RC\) to simplify calculations)

   ![Circuit Diagram](image)

3b. Find the delay to change logic state of Inverter Output (Point X) from 1->0.

4. Problem 1.84b

5. Problem 1.88