HW3

1. Consider a bag comprising of marbles with three distinct colors: black, white and red. A person starts taking out 2 marbles at a time, and obeys the following rules:
   1. If both marbles are red, black or white, puts one back in the bag and removes the other one.
   2. If one is black and the other is white, puts black back and removes white.
   3. If one is black and the other is red, puts black back and removes red.
   4. If one is red and the other is white, puts red back and removes white.

   a) Draw a petri net that models this process. Assume Nr, Nb and Nw red, black and white marbles initially in the bag.
   b) Is this petri net live? Show why?

2. Phase change RAM is a new non-volatile memory technology. What are the primary advantages of using it an alternative memory technology to DRAM? What benefits does PCM bring specifically to embedded systems? Also discuss the challenges in using it as a DRAM replacement.

3. Explain what the following VHDL code is doing. Also draw the corresponding FSM.

```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity rbc is
  port (  
    cout   :out std_logic_vector (3 downto 0);  -- cout
    enable :in  std_logic;                      -- Enable
    clk    :in  std_logic;                      -- Input clock
    reset  :in  std_logic                       -- Input reset
  );
end entity;

architecture rtl of rbc is
  signal iq :std_logic_vector (3 downto 0);
begin
  process (clk, reset) begin
    if (reset = '1') then
      iq <= (others=>'0');
    elsif (rising_edge(clk)) then
      if (enable = '1') then
        iq <= iq + 1;
      end if;
    end if;
  end process;
  cout <= (iq(3) &
          (iq(3) xor iq(2)) &
          (iq(2) xor iq(1)) &
          (iq(1) xor iq(0)));
end architecture;
```
4. We have a set of four independent tasks with equal execution times, but period of each task is twice as the previous one ($T_{i+1} = 2T_i$). In order to make sure that this set of tasks is schedulable with rate monotonic scheduling, determine the possible range of utilizations for the first task.

5. Suppose a processor with two power states $P_{on}=1W$ and $P_{idle}=50mW$. Assume it goes to the idle state as soon as it gets idle. Its shutdown delay (time spent for transition from on to idle state) is 10us and its wakeup delay (time spent for transition from idle to On state) is 90us. During transitions between On and idle states, it consumes 1500mW. It wakes up once a thread arrives that is ready to run. At what length of the idle times does it makes sense for this processor to transition into sleep state?

6. Examine the following Esterel code:

    module Example:
    input A,B,C;
    output O;
    loop
        [ await A || await B ] ;
        emit O;
        await C
    end

   a) Explain what the code is doing.
   b) Draw the FSM that accurately represents the functionality of this code

7. Assume an A/D converter is supplying samples at 44.1 kHz.
   a. How much time is available per sample for CPU operations?
   b. If the interrupt handler executes 100 instructions obtaining the sample and passing it to the application routine, how many instructions can be executed on a 20 MHz RISC processor that executes 1 instruction per cycle?