Post Route Simulation

Open New Project and select Top Level Source Type = HDL

Click Next
Select **Virtex2P** in *Family*

Simulator is **ISE Simulator**

Leave remaining selections unchanged and click next -> next
Click Finish

Add a new source as shown in the diagram above
Select Verilog Module and give a filename

Click Next. You need not give any inputs or outputs here. You can initiate them in your Verilog code.
Complete the Verilog code and add a Test Bench Waveform

Click next
After you are done with your code and you checked the simulation:

To find the delay, Select the **Post-Route Simulation** as shown in the figure above.
Run the Simulate Post-Place & Route Model

Continue as shown in the delay tutorial on the class webpage.