1. a) $Z = 00001000100000100010$
   
   b)

   ![State Transition Diagram]

2. a)
b) 

\[ g_0: \{S_0, S_3\} \]

\[ g_1: \{S_1, S_2, S_5\} \]

\[ g_2: \{S_4\} \]

\[ g_3: \]

\[ g_4: \]

\[ g_5: \]

c) 

<table>
<thead>
<tr>
<th>Present state</th>
<th>Next state</th>
<th>Output Z</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>X=0</td>
<td>X=1</td>
</tr>
<tr>
<td>g0</td>
<td>g2</td>
<td>g1</td>
</tr>
<tr>
<td>g1</td>
<td>g1</td>
<td>g0</td>
</tr>
<tr>
<td>g2</td>
<td>g1</td>
<td>g1</td>
</tr>
</tbody>
</table>
Exercise 9.4

Using the counter from Figure 9.5, we can easily construct this left-right LED design. When the system is reset, we need to start out in state nine. This can be accomplished by hard-wiring the load inputs of the counter to 4, which corresponds to the middle of nine states from 0 to 8, and tying the load input to reset. If we assume that either the left or right input will be asserted at once, never at the same time (or if they are, right will take precedence), then we can tie the right signal to the up input of the counter so that when right is asserted it will advance to the next higher state. ORing the left and right inputs and using that as the enable signal of the counter will ensure that the counter only changes when right or left is asserted. Finally, two gates use the outputs of the counter to set the Left_LED and Right_LED as well as disabling the counter from advancing further. The resulting circuit schematic looks as follows:
4. Next State equations

\[ S_8^{+} = S_8 + S_7L \]
\[ S_7^{+} = S_6L \]
\[ S_6^{+} = S_7R + S_5L \]
\[ S_5^{+} = S_6R + S_4L \]
\[ S_4^{+} = S_5R + S_3L \]
\[ S_3^{+} = S_4R + S_2L \]
\[ S_2^{+} = S_3R + S_1L \]
\[ S_1^{+} = S_2R \]
\[ S_0^{+} = S_1R + S_0 \]

Left LED = \( S_8 \)
Right LED = \( S_0 \)

Use the above equations to implement the PAL connections on the data sheet
Figure 9.28  P22V10 PAL.