HW # 3 SOLUTIONS

1.

**Exercise 3.18**

(a) The K-map for this function shows that there are adjacent groups 1’s without a circle:

\[ F(A,B,C) = A'B + A'C + BC' \]

(c) The K-map for \( F \):

\[ F(A,B,C) = AB' + AC + BC \]
2.

**Exercise 4.10**

(a)

(b)
Exercise 4.13
(b)
Exercise 4.14

(a)

(b)
Exercise 4.18

(a) By simplifying the function, it is realized that $AB'C$ is already covered by $AC$, so $B$ is not needed as an input to the multiplexer.

(b)
Exercise 5.3

(a) Truth table for $O_1$ and $O_0$:

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<thead>
<tr>
<th>$I_3$</th>
<th>$I_2$</th>
<th>$I_1$</th>
<th>$O_1$</th>
<th>$O_0$</th>
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(b) Gate-level implementation:

$O_1 = I_3 + I_2$

$O_0 = I_3 + I_2 \cdot I_1$

(c) 4:1 multiplexor implementation:
Exercise 5.12
The main functionality of the ALU can be broken into four parts: 0, arithmetic, logic, and 1. Each of these is pieces shares functionality. We can use the control signals and small multiplexors to get the correct functionality. The four components come together with a 4:1 multiplexor, which is controlled with some logic that selects the correct input for a given S2-S0 value.

The separate components are grouped together in the following circuit schematic:
Exercise 6.2

Extending this solution to either \( n = 12 \) or \( n = 30 \) inputs requires

\[
\sum_{i=2}^{n} (i - 1)
\]

R-S latches. Where each output would have an AND gate with \( n-1 \) inputs. This would cause significant delay and could be quite noticeable.
Exercise 6.5