

List of Projects, Spring 2008, CK Cheng

1. Parallel Processing: Simulation with distributed processors.

Bottlenecks: LU decomposition is by natural a serial process. Iterative methods may not be able to handle general cases.

References: A.E. Ruehli

2. Statistical Analysis: Monte Carlo analysis

Bottlenecks: Monte Carlo approach requires many runs of various parameter configurations.

References: Quasi-Monte Carlo, R.A. Rutenbar

3. Nonlinear System Solution: DC solution

Bottlenecks: The Newton Raphson method may not converge.

Possible Direction: Homotopy

References: J. Roychowdhury, Hsiao-Dong Chiang, K. Yamamura

4. Power Ground Distribution Analysis

Bottlenecks: Large circuits with long time interval.

Possible Direction: linear networks

References:

Sheldon Tan, S.R. Nassif, Sachin Sapatnekar, E.G. Friedman

5. Clock Distribution Analysis

Bottlenecks: Large circuits

Possible Direction: Tree structure of clock networks

References:

Sheldon Tan, S.R. Nassif, Sachin Sapatnekar, E.G. Friedman

6. Memory: Structured and regular array of cells.

Bottlenecks: High number of cells linked by power ground and signal wires. The circuit complexity is high for post layout simulation.

Direction: Nassda, HSIM,

7. Circuit Reduction

Bottlenecks: High parasitic after post-layout extraction

Possible Direction: Reduction according to circuit structure

References: Star-RCXT