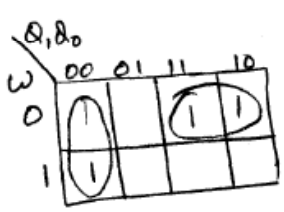
First Name: Last Name: PID:

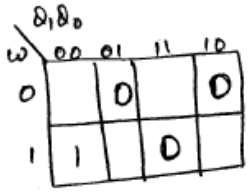
4. (10 points)
An FSM is defined by the following state transition table.

Present State $Q_1 Q_0$	Next state W=0 $Q_1^+ Q_0^+$	Next state W=1 $Q_1^+ Q_0^+$	Output Z
00	10	11	0
01	00	00	0
10	10	00	0
11	10	00	1

(a) Derive the next state and output equations.



K-map for Q_1^+



K-map for Q_0^+

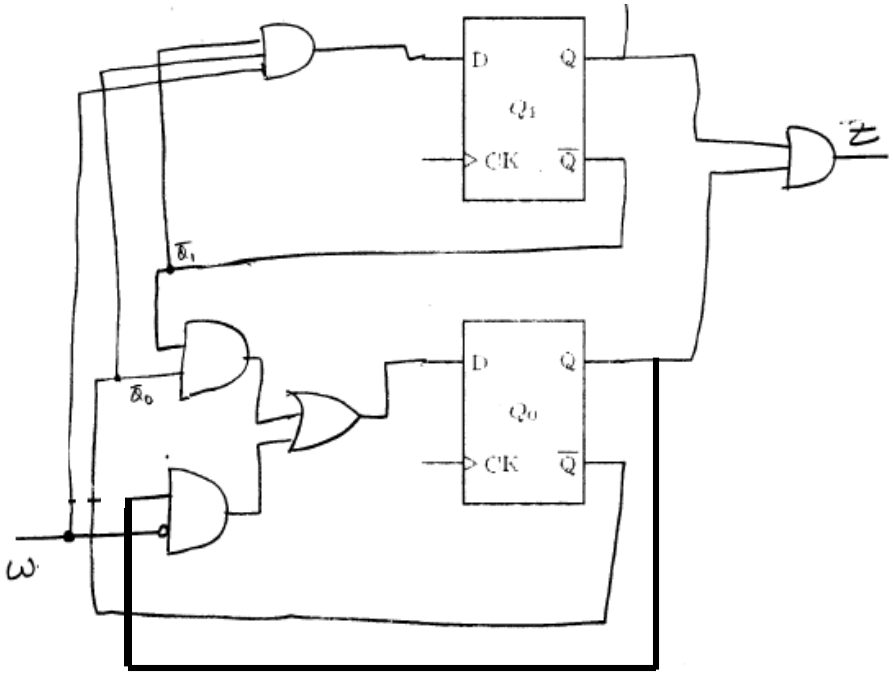
$Q_1^+ = \overline{Q}_1\overline{Q}_0 + Q_1\overline{w}$ $\quad Q_0^+ = \overline{Q_1}\overline{Q_0}\,w$

→Since this is a Moore machine, output depends only on current State

$Z = Q_1 Q_0$

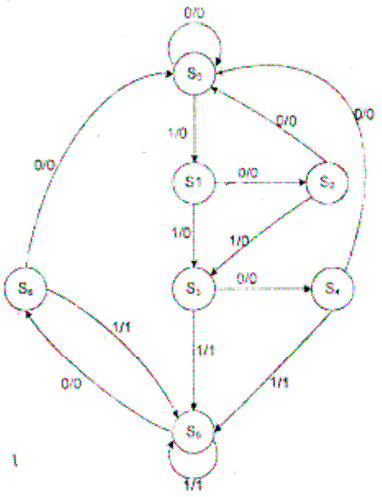
First Name: Last Name: PID:

(b) Provide the logic schematic of this machine using only D flip-flops, AND gates, OR gates, and NOT gates.



First Name: Last Name: PID:

5. Consider the following state diagram:

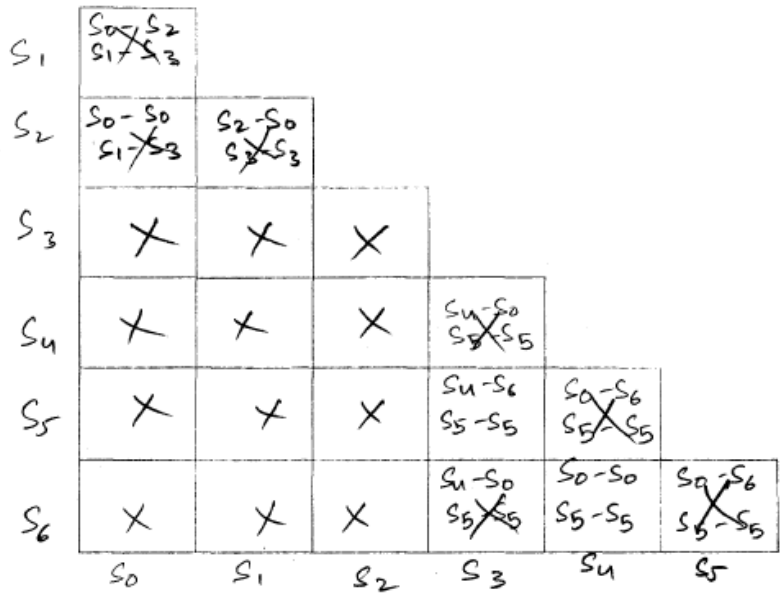


(a) Fill out the blanks in the state table

Present State	Next State		Output Y	
	A = 0	A = 1	A = 0	A = 1
S_0	S_0	S_1	0	0
S_1	S_2	S_3	0	0
S_2	S_0	S_3	0	0
S_3	S_4	S_5	0	1
S_4	S_0	S_5	0	1
S_5	S_6	S_5	0	1
S_6	S_0	S_5	0	1

First Name: Last Name: PID:

(b) Label the rows and columns with states, and then fill the implication table.



(c) List all the original states, grouped into maximal classes of compatibility. Use only as many groups as necessary

$g_0 =$ S_0 ✓

$g_1 =$ S_1 ✓

$g_2 =$ S_2 ✓

$g_3 =$ $\{S_3, S_5\}$ ✓

$g_4 =$ $\{S_4, S_6\}$

$g_5 =$

$g_6 =$

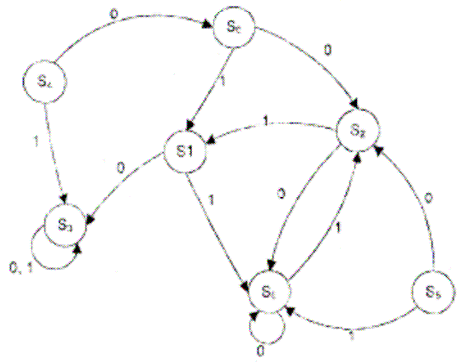
First Name: Last Name: PID:

(d) Show the minimized state transition and output table. Fill in only as many rows of the table as necessary.

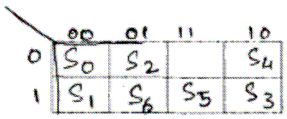
Present State	Next State		Output Y	
	A = 0	A = 1	A = 0	A = 1
g_0	g_0	g_1	0	0
g_1	g_2	g_3	0	0
g_2	g_0	g_3	0	0
g_3	g_4	g_3	0	1
g_4	g_0	g_3	0	1
g_5				
g_6				

First Name: Last Name: PID:

6. Consider the finite state machine shown below.



Implement a state assignment using the minimum bit-change heuristic. Show your result in both K-map and the table.



State Name	Assignment		
	Q_2	Q_1	Q_0
S_0	0	0	0
S_1	0	0	1
S_2	0	1	0
S_3	1	0	1
S_4	1	0	0
S_5	1	1	0
S_6	0	1	1