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CSE 140 Midterm 2
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Fall 2006

- Do not start the exam until you are told to.
- Turn off any cell phones or pagers.
- Write your name and PID at the top of every page. Do not separate the pages.
- This is a closed-book, closed-notes, no-calculator exam. You many only refer to one page of your own notes.
- Do not look at anyone else's exam. Do not talk to anyone but an exam proctor during the exam.
- If you have a question, raise your hand and an exam proctor will come to you.
- You have 80 minutes to finish the exam. When the time is finished, you must stop writing.
- Write your answers in the space provided.
- To get the most partial credit, clearly and neatly show all steps of your work.

1. 10 points	
2. 20 points	
3. 15 points	
4. 20 points	
5. 25 points	
6. 10 points	
Total (100 points)	

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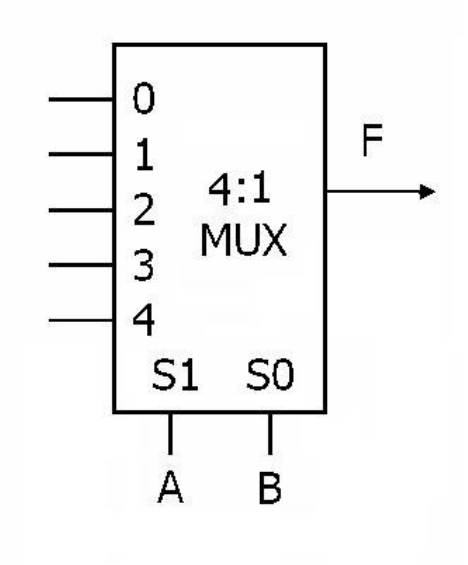
1. **(10 points)**
   Implement the function F using a 4:1 multiplexer shown below.
   $F(A,B,C,D) = \Sigma\ m(5, 6, 7, 8, 11, 12, 13) + d(2, 15)$
   Use minimum number of gates to implement the function.
   You cannot assume that negated values of inputs are available.



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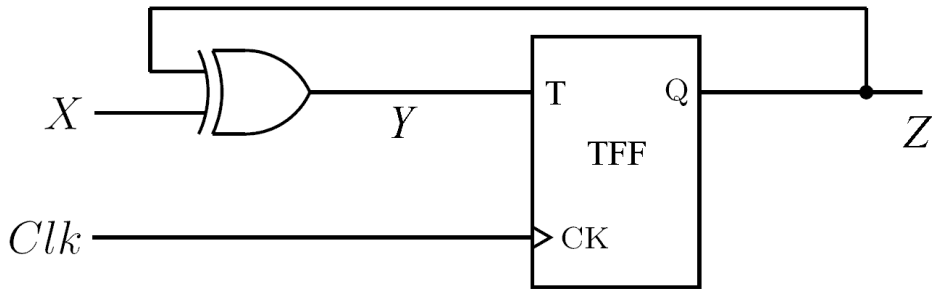
2. **(20 points)**

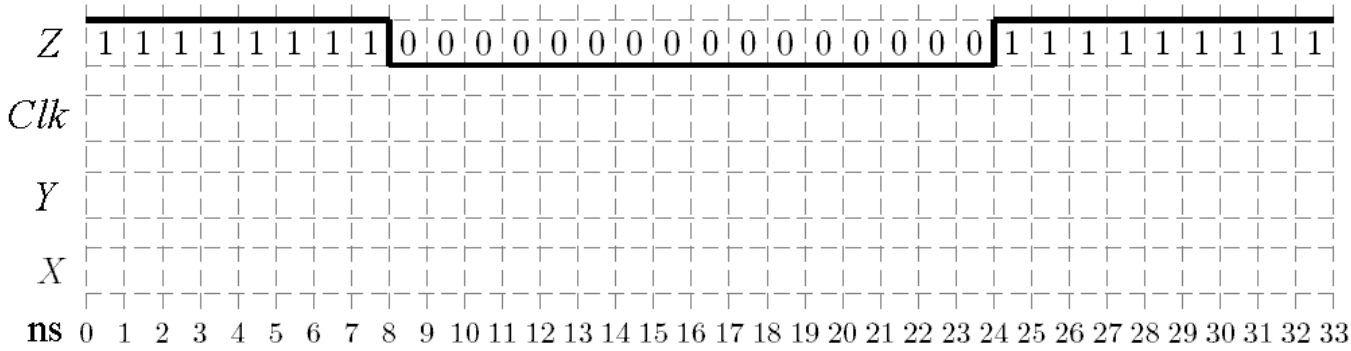
Given the observed output Z below of the circuit given above, determine what the inputs Clk and X must be.

You may make the following assumptions:

- The clock has a period of 8 nanoseconds (ns) and a 25% duty cycle.
- The positive edge-triggered T flip-flop has a setup time T_{su} of 2 ns, a hold time T_h of 1 ns.
- Propagation delay(T_{pd}) through the T flip flop is 3ns and the delay through XOR gate (T_{XOR}) is 1 ns.

If the value must be a 1, write 1. If the value must be 0, write 0. If the value can either be 0 or 1, write X. Avoid unnecessary transitions. If you have the flexibility to change X input at different times, change it at the negative edge of the clock .





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3. (15 points)
A sequential circuit has two inputs w1 and w2, and an output, z. Its function is to compare the input sequences on the two inputs. If w1=w2 during any four consecutive clock cycles, the circuit produces z=1; otherwise, z=0.

For example:
W1: 0110111000110
W2: 1110101000111
Z : 0000100001110
Draw the state diagram using at most 5 states.

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4. (20 points)
An FSM is defined by the following state transition table.

Present State $Q_1 Q_0$	Next state		Output Z
	W=0 $Q_1^+ Q_0^+$	W=1 $Q_1^+ Q_0^+$	
00	10	11	0
01	00	00	0
10	10	00	0
11	10	00	1

(a) Derive the next state and output equations.

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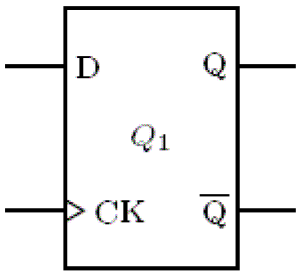
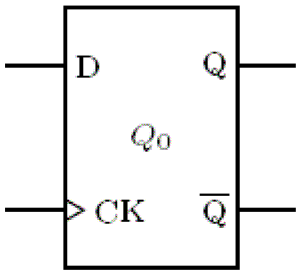
(b) Provide the logic schematic of this machine using only D flip-flops, AND gates, OR gates, and NOT gates.





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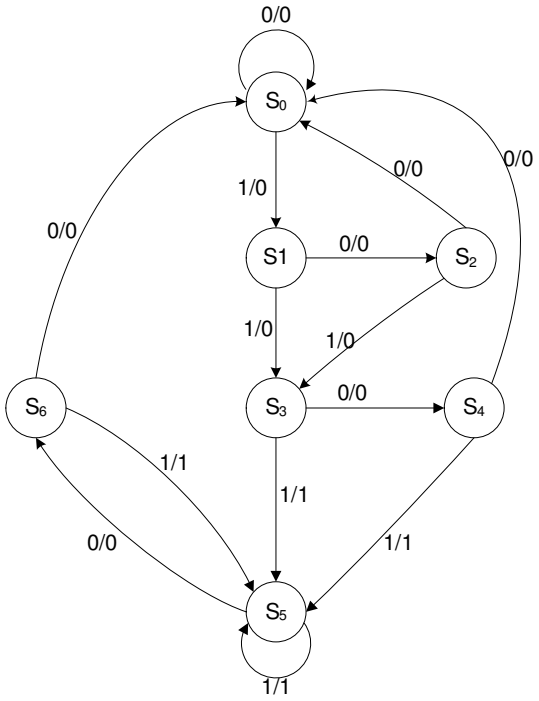
5. (25 marks) Consider the following state diagram:



(a) Fill out the blanks in the state table

Present State	Next State		Output Y	
	A = 0	A = 1	A = 0	A = 1
S_0	S_0	S_1	0	0
S_1	S_2	S_3	0	0
S_2	S_0	S_3	0	0
S_3	S_4	S_5		
S_4	S_0		0	
S_5				
S_6		S5		1

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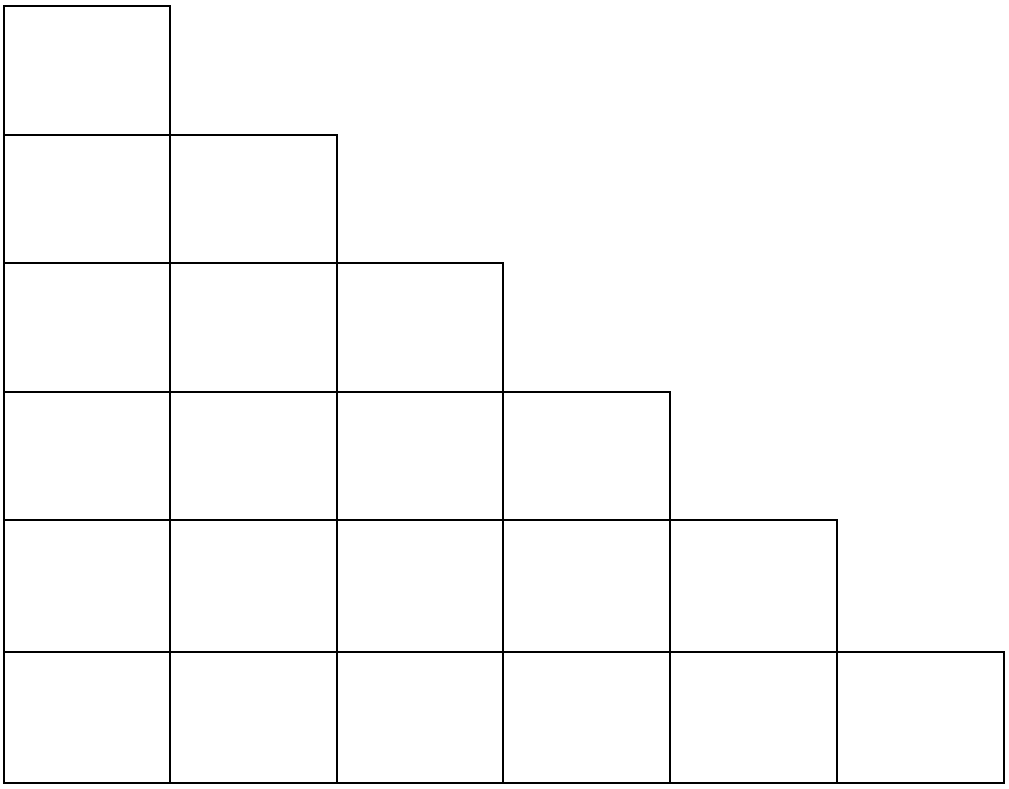
(b) Label the rows and columns with states, and then fill the implication table.



S_0

(c) List all the original states, grouped into maximal classes of compatibility. Use only as many groups as necessary.

g_0 = _____

g_1 = _____

g_2 = _____

g_3 = _____

g_4 = _____

g_5 = _____

g_6 = _____

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(d) Show the minimized state transition and output table. Fill in only as many rows of the table as necessary.

Present State	Next State		Output Y	
	A = 0	A = 1	A = 0	A = 1
g_0				
g_1				
g_2				
g_3				
g_4				
g_5				
g_6				

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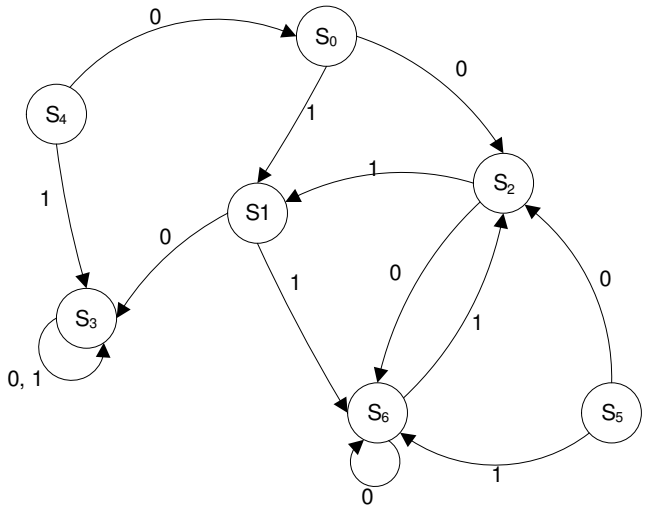
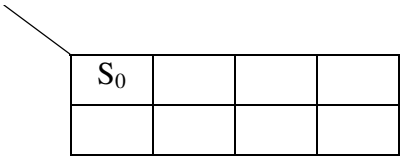
6. (10 marks) Consider the finite state machine shown below.



Implement a state assignment using the minimum bit-change heuristic. Show your result in both K-map and the table.



State Name	Assignment		
	Q_2	Q_1	Q_0
S_0			
S_1			
S_2			
S_3			
S_4			
S_5			
S_6			

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