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CSE 140 Midterm 2
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Spring 2008

- Do not start the exam until you are told to.
- Turn off any cell phones or pagers.
- Write your name and PID at the top of every page. Do not separate the pages.
- This is a closed-book, closed-notes, no-calculator exam. You many only refer to one page of your own handwritten notes.
- Do not look at anyone else's exam. Do not talk to anyone but an exam proctor during the exam.
- If you have a question, raise your hand and an exam proctor will come to you.
- You have 80 minutes to finish the exam. When the time is finished, you must stop writing.
- Write your answers in the space provided.
- Clearly and neatly show all of the steps of your work to get the most partial credit

1. 10 points	
2. 10 points	
3. 20 points	
4. 15 points	
5. 15 points	
6. 15 points	
7. 15 points	
8. 10 points	
Total 100 points (+10 bonus)	

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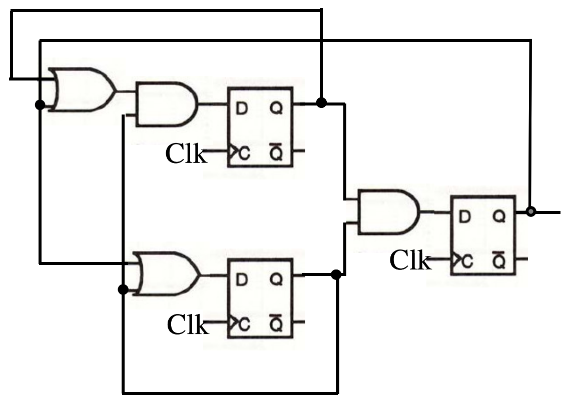
Problem 1. (10 points)
Determine the maximum frequency of the clock, given:

T_{setup} = 2ns
T_{pd} = 2ns
T_{hold} = 1.5ns
$T_{AND/OR}$ = 1ns (AND/OR gates delay)



Solution:
Critical path: OR -> AND -> D-FF:

$T_{period} > T_{pd} + T_{OR} + T_{AND} + T_{setup}$ = 2+1+1+2=6ns

Frequency < 1/6ns

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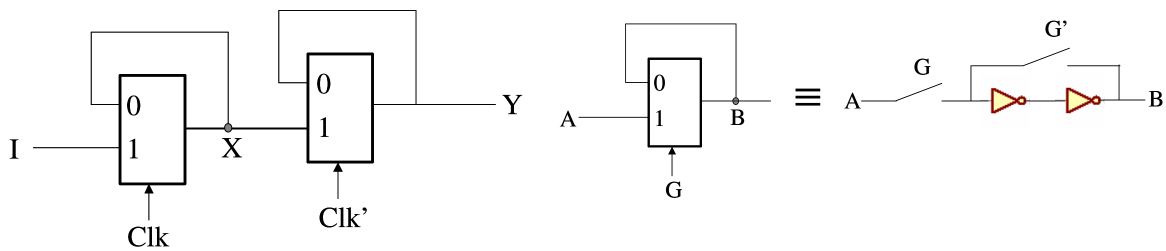
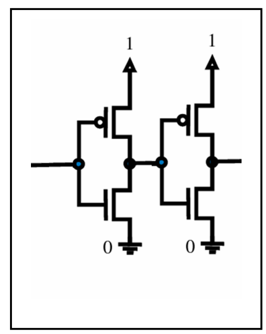
Problem 2. (10 points)

(a) Determine the worst-case delay between the points *X* and *I* for the circuit below in terms of nMOS resistance, *Rn*, and gate capacitance *Cg*. Assume *Rp=2Rn*.



Solution:

The delay at X = 6RnCg



(b) What does this circuit do?

Solution:

Negative edge triggered Master-slave D flip-flop

Problem 3. (20 points)

A Mealy machine has one input *X* and one output *Z*. Given the following state transition table, use the *implication chart method* to minimize the number of states.

Present State	Next State		Output Y	
	X = 0	X = 1	X = 0	X = 1
S_0	S_1	S_4	0	0
S_1	S_2	S_1	0	0
S_2	S_1	S_6	0	0
S_3	S_1	S_3	0	0
S_4	S_5	S_4	0	0
S_5	S_2	S_1	0	0
S_6	S_5	S_3	0	1

Solution:

a) Label the rows and columns with states, and then fill the implication chart

	S0	S1	S2	S3	S4	S5
S1	~~S1=S2 S1=S4~~					
S2	~~S1=S1 S4=S6~~	~~S1=S2 S1=S6~~				
S3	S1=S1 S3=S4	~~S1=S2 S1=S3~~	~~S1=S1 S3=S6~~			
S4	S1=S5 S4=S4	~~S2=S5 S1=S4~~	~~S1=S5 S4=S6~~	S1=S5 S3=S4		
S5	~~S1=S2 S1=S4~~	S2=S2 S1=S1	~~S1=S2 S1=S6~~	~~S2=S1 S1=S3~~	~~S2=S5 S1=S4~~	
S6	X	X	X	X	X	X

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Problem 3. cont..

b) Show the Maximal Class of Compatibility. Fill in as many groups as necessary.

g0:_{S0, S3,S4}_
g1:_{S1,S5}____
g2:_{S2}_______
g3:_{S6}_______
g4:____________
g5:____________
g6:____________

c) Identify a set that satisfies both covering and closure conditions on minimal class of compatibility. List the resulting state transitions and outputs in a table. Fill in as many rows of the table as necessary.

Present State	Next State		Output Y	
	X = 0	X = 1	X = 0	X = 1
g0	g1	g0	0	0
g1	g2	g1	0	0
g2	g1	g3	0	0
g3	g1	g0	0	1
g4				
g5				
g6				

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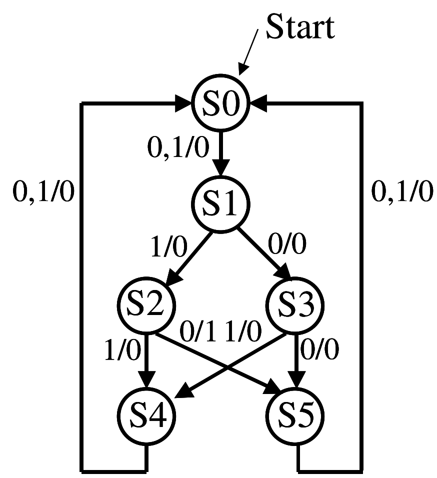
Problem 4. (15 points)

Implement a state assignment using three guidelines based on next state and input/outputs for the state diagram below.



Solution:

Highest priority states: 2 (S4, S5), 2 (S2, S3)
Medium priority states: S2, S3
Lowest priority states: 0/0: {S0, S1, S3, S4, S5}
1/0: {S0, S1, S2, S3, S4, S5}

Q2 \ Q1Q0

S0	**S3**	**S4**	**S1**
	S2	**S5**	

*It should be noted that alternative solutions could exist

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Problem 5. (15 points)

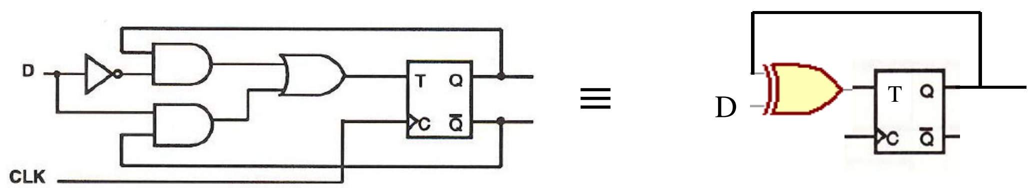
(a) Design a basic cell of a universal shift register that satisfies the following:

- Uses a positive edge-triggered *T-flip flops* as internal storage
- Has two select bits, S_0 and S_1, to determine the shift function as follows:

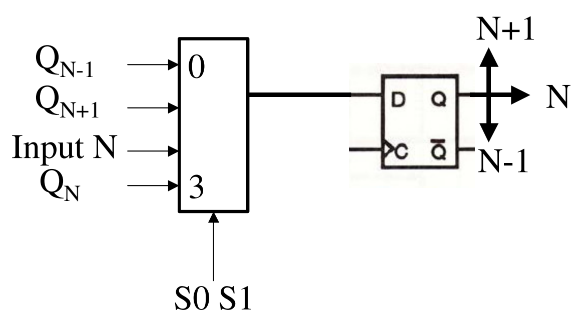
S_0	S_1	Function
0	0	Shift left
0	1	Shift right
1	0	Load new value
1	1	Hold the state

Solution:

First we need to implement a D-FF from a T-FF as follows:



Then we use the D-FF to implement the basic cell of the universal shift register as follows:

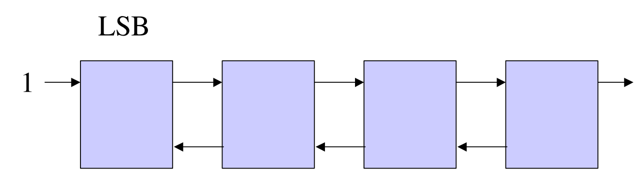


Problem 5. cont..

(b) Construct a circuit to perform the operation of *multiplying a 4-bit number by 2 and adding 1* using the basic cell of part (a) with NO additional logic gates.

We perform that through the use of a shift register structure, shift right, and inserting a 1 at the LSB side

2 * X1 X2 X3 X4 +1 = X2 X3 X4 1



The function need to be set to shift right

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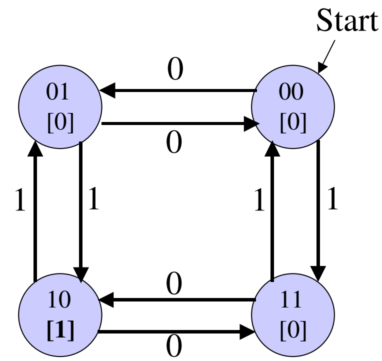
Problem 6. (15 points)
Design a minimum state FSM that gives 1 as output if the total number of both 0's and 1's received is <u>odd</u>, otherwise it outputs 0. Draw its diagram.

Solution:



State 00: Even #0's & even #1's
State 01: Odd #0's & even #1's
State 10: Odd #0's & odd #1's
State 11: Odd #1's & even #0's

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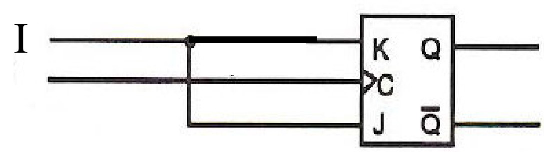
Problem 7. (15 points)
Using the following state transition table, implement the next state output, *S1+*, using *J-K flip-flops* with minimal logic gates.

I (Input)	Current state S1	S0	Next state S1+	S0+	Output
0	0	0	0	1	0
0	0	1	0	0	0
0	1	0	1	1	0
0	1	1	1	0	1
1	0	0	1	1	0
1	0	1	1	0	1
1	1	0	0	1	0
1	1	1	0	0	0

Solution:
Using K-map, the functions of J and K that are required to implement S1+ are shown in the following:

$K^+ = I$
$J^+ = I$



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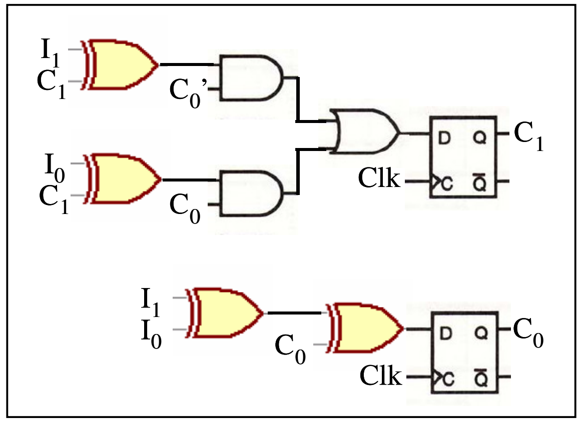
Problem 8. (BONUS) (10 points)
Draw the state diagram implemented by the circuit below. What does this circuit do?



Solution:

I1	I0	C1	C0	C1+	C0+
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	1	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	0	1	0	0
1	0	1	0	0	1
1	0	1	1	1	0
1	1	0	0	1	0
1	1	0	1	1	1
1	1	1	0	0	0
1	1	1	1	0	1

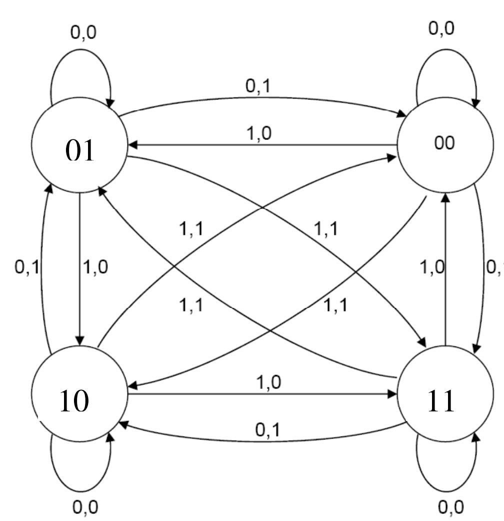
Stop counting

Count up by 1

Count down by 1

Count up by 2

I0, I1



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