

# Lab 1c Review

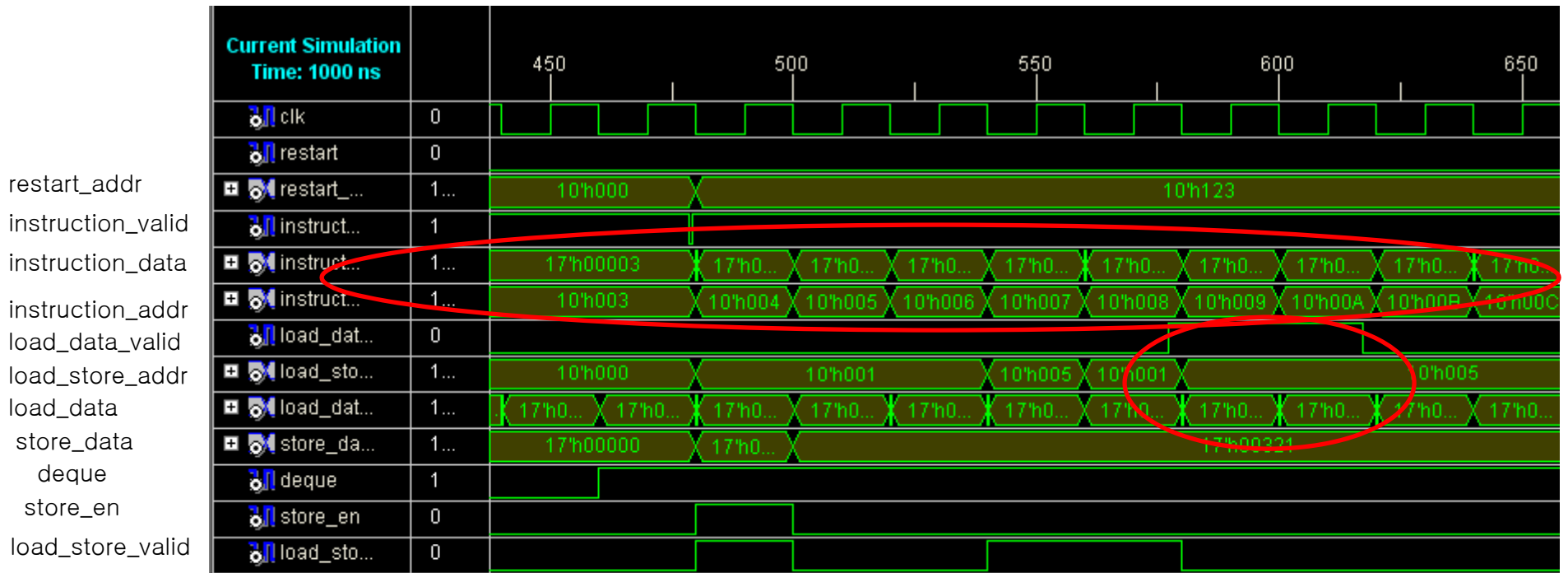
CSE141L

4/30

# Announcements

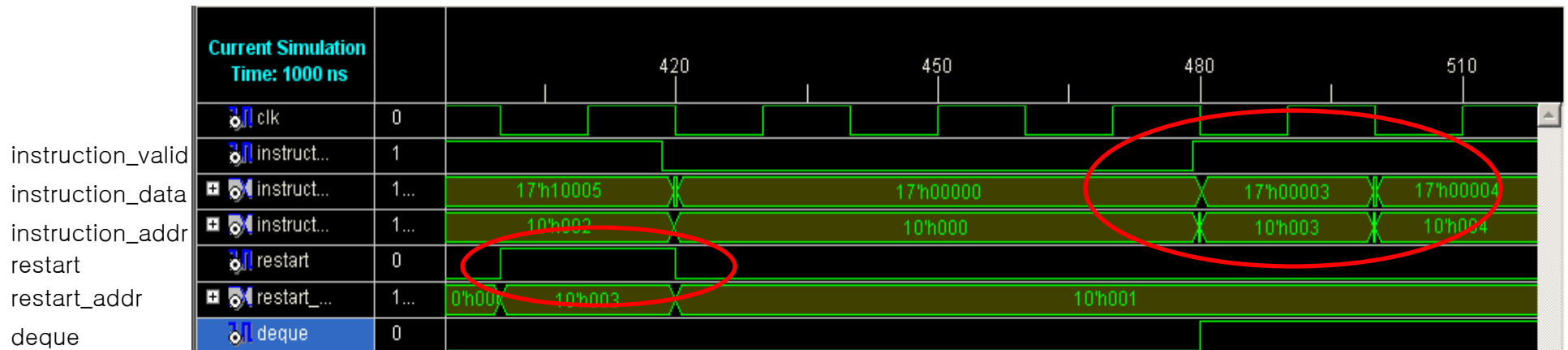
- Sign up for teams!
  - Only 8 people have signed up so far..
- Lab 1c amnesty policy
  - 85% credit if submitted by next Monday
- Lab 2a
  - 5/2(W)
    - email draft of your manual and list of your team members
  - 5/4(F)
    - email revised draft of your manual and one benchmark
  - 5/11(F)
    - lab 2a + lab2b together (hardcopy + email)

# test.tfw



- Is a fetch unit affected by load or store operations?

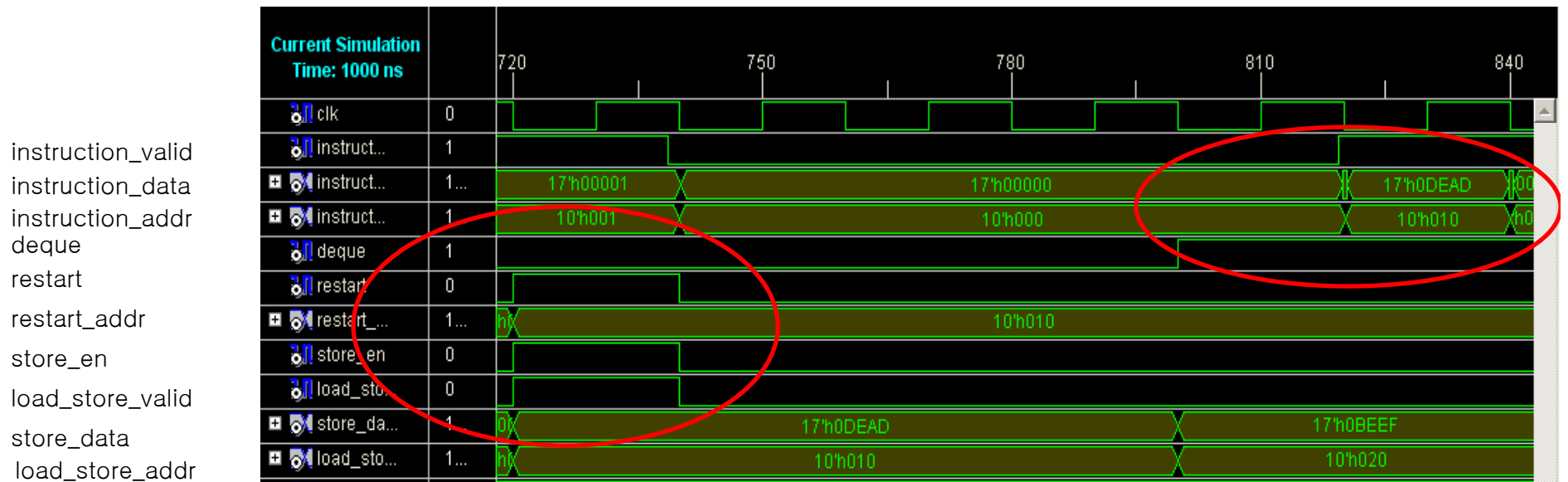
# branch.tfw



- Note how 'instruction\_valid' changes
- jump vs branch?

```
addr instruction
#0 nonbranch_op0
#1 nonbranch_op1
#2 conditional branch to #7
   (predicted taken)
#3 nonbranch_op3
#4 nonbranch_op4
#5 nonbranch_op5
#6 nonbranch_op6
#7 branch to #0
```

# full.tfw



- Simultaneously assert
  - ‘restart’ from 0x10
  - store ‘0xDEAD’ at 0x10

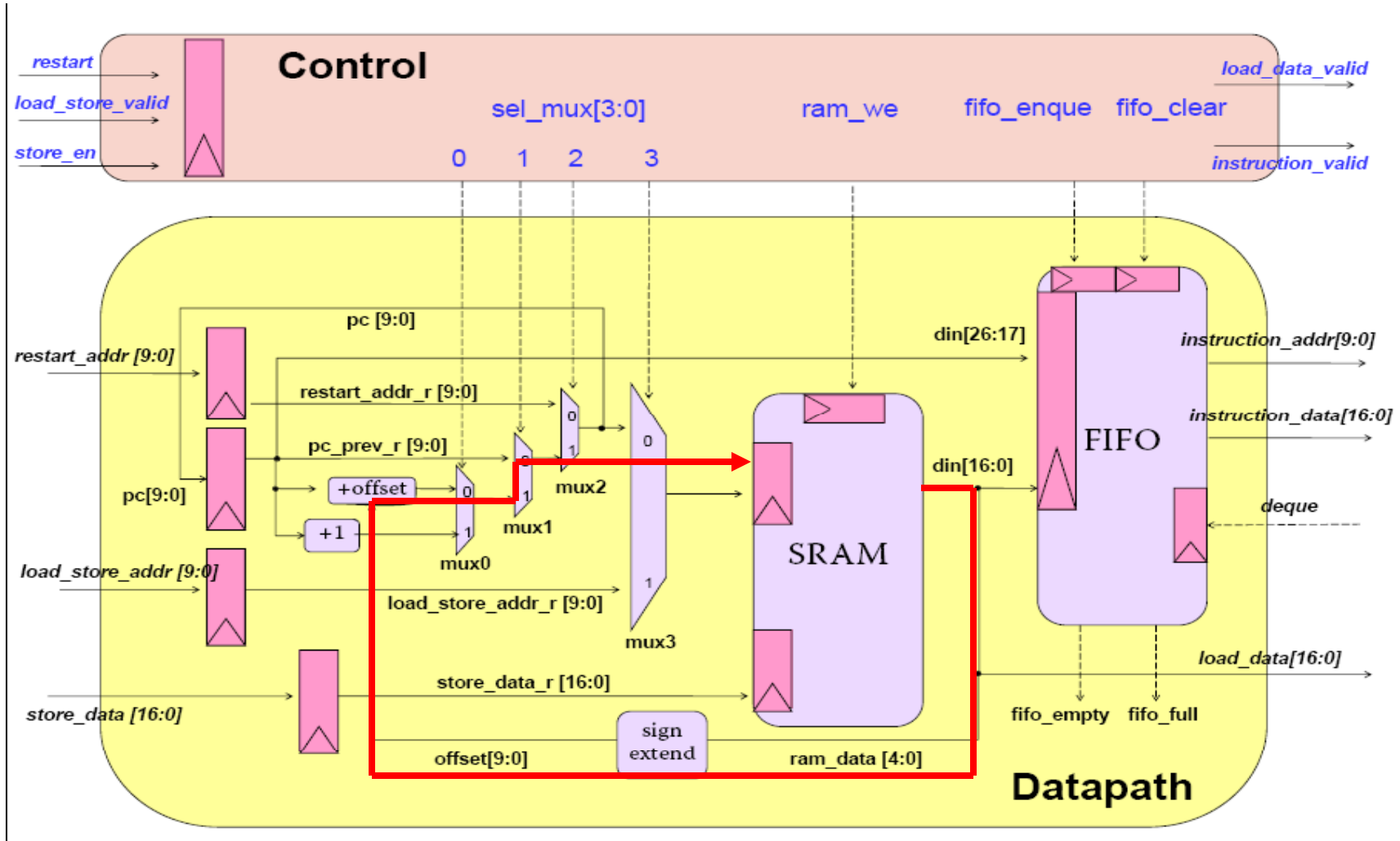
# Implementation Result

Maximum Data Path: ram/BUS to ram/BUS

Delay type	Delay(ns)	Logical Resource
<a href="#">Trcko_DQWA</a>	1.647	<a href="#">ram/BUS</a>
net (fanout=3)	0.523	<a href="#">load_data_2_OBUF</a>
<a href="#">Topcyf</a>	0.435	<a href="#">offset_addr/Madd_dout_lut&lt;2&gt;</a> <a href="#">offset_addr/Madd_dout_cy&lt;2&gt;</a> <a href="#">offset_addr/Madd_dout_cy&lt;3&gt;</a>
net (fanout=1)	0.000	<a href="#">offset_addr/Madd_dout_cy&lt;3&gt;</a>
<a href="#">Tbvp</a>	0.068	<a href="#">offset_addr/Madd_dout_cy&lt;4&gt;</a> <a href="#">offset_addr/Madd_dout_cy&lt;5&gt;</a>
net (fanout=1)	0.000	<a href="#">offset_addr/Madd_dout_cy&lt;5&gt;</a>
<a href="#">Tbvp</a>	0.068	<a href="#">offset_addr/Madd_dout_cy&lt;6&gt;</a> <a href="#">offset_addr/Madd_dout_cy&lt;7&gt;</a>
net (fanout=1)	0.000	<a href="#">offset_addr/Madd_dout_cy&lt;7&gt;</a>
<a href="#">Tciny</a>	0.391	<a href="#">offset_addr/Madd_dout_cy&lt;8&gt;</a> <a href="#">offset_addr/Madd_dout_xor&lt;9&gt;</a>
net (fanout=1)	0.441	<a href="#">offset_out&lt;9&gt;</a>
<a href="#">Tif5</a>	0.341	<a href="#">mux2/dout&lt;9&gt;_1</a> <a href="#">mux2/dout&lt;9&gt;_f5</a>
net (fanout=1)	0.000	<a href="#">mux2/dout&lt;9&gt;_f5</a>
<a href="#">Tif6y</a>	0.292	<a href="#">mux2/dout&lt;9&gt;_f6/MUXF6</a>
net (fanout=1)	0.429	<a href="#">pc&lt;9&gt;</a>
<a href="#">Tilo</a>	0.146	<a href="#">mux3/dout&lt;9&gt;_1</a>
net (fanout=1)	0.403	<a href="#">ram_addr&lt;9&gt;</a>
<a href="#">Trcck_ADDR_A</a>	0.333	<a href="#">ram/BUS</a>
<b>Total</b>	<b>5.517ns</b>	<b>(3.721ns logic, 1.796ns route) (67.4% logic, 32.6% route)</b>

- 5.517ns Cycle Time
- 181.26MHz
- How many instructions per second?

# The Critical Path





# Any Questions?

- Lab 1c
- Lab 2a