Lab 1b Q & A

CSE141L

4/16/2007
Lab 1b

- Datapath Updated
Various Verilog Styles

• Behavioral (Functional) Verilog
  – Maybe not synthesizable
  – Only use for testbenches

• RTL Verilog
  – Synthesizable
  – Commonly used for control logic implementation

• Structural Verilog
  – “Synthesizable”
  – ‘instantiate’ and ‘wire up’ modules
  – Commonly used for datapath implementation
module fetch  
(  
    input clk,  
    input ......  
    output ......  
);  
mod1#(10) ins1 (.sel(sel_mux[0]), ...........);  
mod2#(1,2) ins2 (.sel(sel_mux[1]),............);  
..........  
always @( posedge clk )  
begin  
a <= b;  
........  
end  
endmodule

- Use structural verilog
- You might use non-blocking assignments for flip-flops.
module something
(
    input[3:0] a,
    input[3:0] b,
    output ......
);

assign out = a + b;

always @( posedge clk )
begin
    c <= b + e;
    ........
end
endmodule

• Use RTL verilog
• You can use anything synthesizable.
Any Question?
Lab 1a Statistics

Average: 83.16
Behavioral vs Postroute Simulation

- Behavioral Simulation

- Postroute Simulation
Xilinx Delay Estimation

- **Synthesis**
  - Use wireload model to estimate wire delay
  - Logic: 1.19
  - Wire: 0.554
  - Inaccurate

- **Map**
  - No routing information
  - Logic: 1.782
  - Wire: 0
  - Inaccurate

- **PostRoute**
  - Use accurate routing information
  - Logic: 1.735
  - Wire: 1.897
  - Accurate
Any Question?