Lab 1c Discussion

4/18/2007

CSE141L
In Lab 1b...

- Understand requirements for the fetch unit
- Implement the provided datapath in the structural verilog
In Lab 1c...

• Complete control logic in the fetch unit
• Validate your design with provided testbenches via post-route simulations
What is the role of a flip-flop?

- Storage? Maybe...

- Control the progress of a signal!
Escapement Strategy

The Solution:
Add two gates
and only open
one at a time.

Source: Chris Terman’s class slides in 6.004, MIT
Single-clock Synchronous Circuits

We’ll use Flip Flops and Registers – groups of FFs sharing a clock input – in a highly constrained way to build digital systems:

**Single-clock Synchronous Discipline**

- No combinational cycles
- Single clock signal shared among all clocked devices
- Only care about value of combinational circuits just before rising edge of clock
- Period greater than every combinational delay
- Change saved state after noise-inducing logic transitions have stopped!

Source: Chris Terman’s class slides in 6.004, MIT
Post Route Simulation

<table>
<thead>
<tr>
<th>clk</th>
<th>mem_addr[9:0]</th>
<th>load_data[16:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>10h007</td>
<td>17h00006</td>
</tr>
<tr>
<td>1</td>
<td>10h000</td>
<td>17h10019</td>
</tr>
</tbody>
</table>


Flip Flop Timing - I

$t_{PD}$: maximum propagation delay, CLK $\rightarrow$ Q

$t_{CD}$: minimum contamination delay, CLK $\rightarrow$ Q

$t_{SETUP}$: setup time

*guarantee that $D$ has propagated through feedback path before master closes*

$t_{HOLD}$: hold time

*guarantee master is closed and data is stable before allowing $D$ to change*

Source: Chris Terman’s class slides in 6.004, MIT
FIFO Interface

• **deque**
  – Please get rid of the current item

• **instruction_valid**
  – The output of FIFO is valid

• Timing diagram?
Lab 1c

• Due: 4/25

• Coming Soon!