Given a four-input Boolean function \( f(a, b, c, d) = \sum m(6, 7, 8, 9, 14) + \sum d(0, 10, 13) \).

a. Implement the function using a minimal network of 2:4 decoders and OR gates.
b. Implement the function using a minimal network of 4:1 multiplexers.
c. Implement the function using a minimal network of 2:1 multiplexers.

II. A sequential adder inputs \( a_i, b_i \), the \( i \)'th bit of two binary numbers in each clock cycle for \( i = 0 \) to \( n - 1 \) and outputs the sum. Implement the adder with a JK flip-flop, a 2-input decoder, and a minimal AND-OR-NOT network (if the network is needed). Draw the schematic diagram.

III. Design a counter with a repeated output sequence 15, 0, 1, 9, 10, 11, 3, 4, with a modulo-16 counter and a minimal combinational network. Write the Boolean expression and draw the schematic diagram.

IV. System Designs:

Implement the following algorithm:
\[ \text{Alg}(X, Y, Z, \text{start}, U); \]
Input \( X[7:0], Y[7:0], Z[7:0], \text{start}; \)
Output \( U[7:0], \text{done}; \)
Local-object \( A[7:0], B[7:0], C[7:0]; \)
S1: If start' goto S1;
S2: done\( <= 0 \) || A\( <= X \) || B\( <= Y \) || C\( <= Z; \)
S3: A\( <= \text{Add}(A, B) || C\( <= \text{Inc}(C) \); \)
S4: A\( <= 2 \times A \) || If C\( [7] \) goto S3;
S5: If A\( [7] \) goto S3;
S6: U\( <= A \) || done\( <= 1 \) || goto S1
End Alg

IV(1). Design a data subsystem that is adequate to execute the algorithm. Draw the schematic diagram to show the design.

IV(2). Design the control subsystem (i) draw the state diagram; (ii) draw the logic diagram that implements the control subsystem with a one hot encoding design.